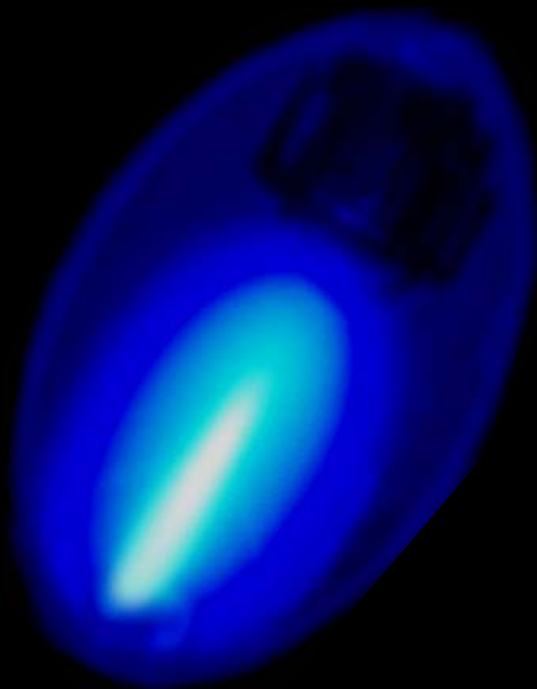


CeO<sub>2</sub> and HfO<sub>2</sub> High-κ Gate Dielectrics  
by Pulsed Laser Deposition  
from binary oxides to nanolaminates



Koray Karakaya



CeO<sub>2</sub> and HfO<sub>2</sub> High-*k* Gate Dielectrics  
by Pulsed Laser Deposition:  
from binary oxides to nanolaminates

*in memoriam Prof. Dr. Adnan Tekin*

**Cover:** The plasma plume formed during pulsed laser deposition. The ablation process takes place in a vacuum chamber. A high energy laser beam hits a solid target material and creates a plasma plume by evaporating the target surface. The plasma plume, which consists of energetic particles, condensates on the substrate surface placed opposite of the target and forms the thin film. The picture is by using the photo taken by Dr. Lianne Doeswijk.

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The research was financially supported by **PHILIPS**

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CeO<sub>2</sub> and HfO<sub>2</sub> High-*k* Gate Dielectrics by Pulsed Laser Deposition: from binary oxides to nanolaminates, Ph.D. thesis University of Twente, Enschede, the Netherlands  
ISBN: 90-365-2353-2

Printed by Wöhrmann Print Service, Zutphen

© Koray Karakaya, 2006

CeO<sub>2</sub> AND HfO<sub>2</sub> HIGH-*K* GATE DIELECTRICS  
BY PULSED LASER DEPOSITION:  
FROM BINARY OXIDES TO NANOLAMINATES

PROEFSCHRIFT

ter verkrijging van  
de graad van doctor aan de Universiteit Twente,  
op gezag van de rector magnificus,  
prof. dr. W.H.M. Zijm,  
volgens besluit van het College voor Promoties,  
in het openbaar te verdedigen  
op donderdag 20 april 2006 om 15.00 uur

door

**Koray Karakaya**

geboren op 1 januari 1973  
te Salihli, Turkije

Dit proefschrift is goedgekeurd door de promotor prof. dr. ing. D.H.A. Blank en de  
assistent promotor dr. ing. A.J.H.M. Rijnders.

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# *Chapter 1*

## **Introduction**

### **Abstract**

Scaling trends in semiconductor technology and the need for high- $k$  gate dielectrics in novel semiconductor devices are summarized. The selection criteria for high- $k$  materials, the role of pulsed laser deposition in materials research activities and other major points in this thesis are presented.

## 1.1. Need for High- $k$ Gate Dielectric Materials

Scaling trends of integrated circuits are defined in 1965 by G. E. Moore in his famous article [1] and known after as ‘Moore’s Law’. Moore’s Law predicts the number of transistors on an integrated circuit will be doubled in each 24 months<sup>1</sup>. This is considered as a self fulfilling prophecy as the semiconductor industry accepted this scaling trend as a roadmap and set their goals accordingly. It explains how integrated device complexity increases by time in order to meet the goals for performance and device costs [2].

The need for high- $k$  gate dielectrics has been emphasized in numerous scientific reports [3, 4]. The gate capacitance is one of the key factors for determining Metal Oxide Semiconductor Field Effect Transistor (MOSFET) performance [5]. The gate capacitance in scaled MOSFETs has to be kept high for good control of the inversion charge by the gate voltage. For a high capacitance with smaller area, decreasing the dielectric thickness or increasing the dielectric constant is needed according to the parallel plate capacitor relation, which is defined as;

$$C = \frac{Ak\epsilon_0}{t_{ox}} \quad (1.1)$$

where,  $C$  is the capacitance,  $A$  is capacitor area<sup>2</sup>,  $t_{ox}$  is the oxide thickness,  $\epsilon_0$  is permittivity of free space and  $k$  is the relative dielectric constant of oxide.

State of the art gate dielectrics ( $\text{SiO}_2$  or  $\text{SiON}$ ) with low dielectric constants show unacceptably high leakage currents. Therefore an oxide layer that is thicker than direct tunneling limit is compulsory to meet the leakage current requirements [3]. In other words, for a given oxide thickness, there is no other way than using high dielectric constant, *i.e.* high- $k$ , materials for maintaining the high capacitance level.

The  $\text{SiO}_2$  (with a  $k$  value of 3.9) equivalent oxide thickness (EOT) of high- $k$  dielectric materials can be written as;

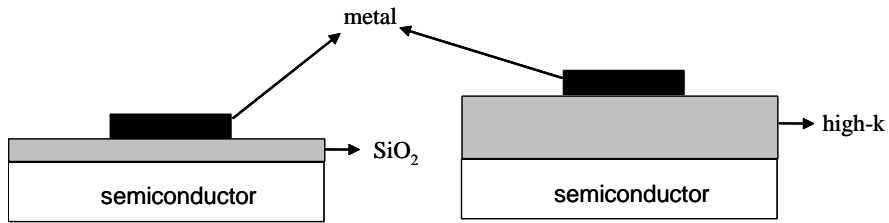
$$EOT = t_{high-k} \frac{3.9}{\kappa_{high-k}} \quad (1.2)$$

where,  $\kappa_{high-k}$  is relative dielectric constant of dielectric with a physical thickness of  $t_{high-k}$ . Figure 1.1 illustrates how the dielectric layer thickness changes by replacing  $\text{SiO}_2$  with a high- $k$  material with the same EOT. Increased physical thickness is the key for the leakage current reduction with high- $k$  materials.

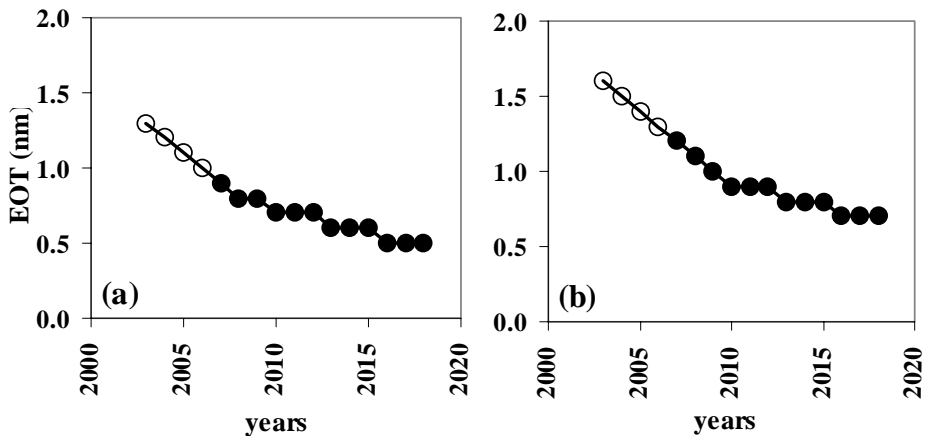
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<sup>1</sup> In the original version, time frame for doubling the complexity of an integrated circuit has been given as 18 months. G.E. Moore changed it to 24 months in 1975.

<sup>2</sup> Area in the parallel plate capacitor corresponds to the gate area of MOSFET.



**Figure 1.1:** Illustration of two MOS devices with  $\text{SiO}_2$  (left) and with high- $k$  dielectric (right), which has the same EOT with the other one (not in scale).



**Figure 1.2:** ITRS projections for EOT of gate dielectrics, for high performance (a), and for low power (b) applications. Full circles indicate where manufacturable solutions for EOT requirement are not known yet.

The need for high- $k$  gate dielectrics is projected as one of biggest near and long term challenges in Industrial Technology Roadmap for Semiconductors (ITRS), and EOT requirements in ITRS are shown in Figure 1.2, for high performance and low power applications according to the 2004 update [6, 7].

## 1.2. High- $k$ Dielectric Materials

Integration of high- $k$  gate dielectrics to silicon technology is a demanding task after the success of  $\text{SiO}_2$  gate dielectrics, which has two main advantages comparing to the other oxides: Large band-gap ( $\sim 9$  eV), which gives excellent leakage current properties *and* high quality interface with silicon, compared to the other oxides on silicon [8-10].

The requirements for high- $k$  dielectric materials have been described in details in literature [3, 4, 11-13] can be summarized as follows:

- Permittivity and barrier height ( $\sim 4$ -5 eV)
- Thermodynamic stability on silicon

- High interface quality
- Layer morphology (amorphous or single crystal)
- Gate compatibility
- Process Compatibility
- Reliability

The thermodynamic stability on silicon, which is one of the most critical requirements for high- $k$  dielectrics, has been described extensively [11, 14-16]. Combining the thermodynamical properties with other requirements, in particular permittivity and band gap [17-20] numerous materials have been investigated as high- $k$  gate dielectric candidates. Among these,  $\text{Al}_2\text{O}_3$  with the large band gap (8.8 eV) provides a good thermodynamic stability on silicon<sup>3</sup>. However,  $\text{Al}_2\text{O}_3$  has low permittivity of ( $k=9$ ) compared to the other high- $k$  candidates.  $\text{HfO}_2$  has received major attention because of its moderate band gap (6 eV), high permittivity ( $k=25$ ), high thermal stability and good process compatibility. However it has lower thermodynamical stability on silicon<sup>4</sup> than  $\text{Al}_2\text{O}_3$ . Another promising candidate is cerium oxide. This material has two common stoichiometry as  $\text{CeO}_2$  and  $\text{Ce}_2\text{O}_3$ , with different thermodynamical stabilities on silicon<sup>5</sup> and different electrical properties as well.

$\text{Ce}_2\text{O}_3$  is one of the best thermodynamically stable materials on silicon. However, has a relative permittivity of  $k=7$ , where  $\text{CeO}_2$  has  $k=26$  [11]. Another advantage of  $\text{CeO}_2$ , in fluorite structure, is its very low lattice mismatch (0.35 %) with silicon, which is an advantage for epitaxial dielectrics for future applications. Its band gap of a 5.5 eV also meets the requirements for high- $k$  dielectrics [21, 22 and 23]. In this thesis  $\text{CeO}_2$  and  $\text{HfO}_2$  are the main interest and their growth and interactions in laminated structures are investigated.

### 1.3. Deposition of High- $k$ Dielectrics

The methods used for deposition of high- $k$  gate dielectrics are explained in details in literature [24-27]. Each deposition method has its own strengths and weaknesses in manner of achieving good electronic properties in layers deposited and excellence in layer uniformity.

Various deposition methods have been reported in literature for growth of  $\text{CeO}_2$  and  $\text{HfO}_2$  layers on silicon: Sputtering [28-35], e-beam evaporation [36-50], chemical vapor deposition (CVD) based methods (Atomic Layer Deposition - ALD, metal-organic CVD) [51-55], molecular beam epitaxy (MBE) [56, 57] and pulsed laser

---

<sup>3</sup>  $\text{Al}_2\text{O}_3$ :  $\Delta G_{1000}=+63.399$  kcal/mol

<sup>4</sup>  $\text{HfO}_2$ :  $\Delta G_{1000}=+47.648$  kcal/mol

<sup>5</sup>  $\text{CeO}_2$ :  $\Delta G_{1000}=+36.290$  kcal/mol -  $\text{Ce}_2\text{O}_3$ :  $\Delta G_{1000}=+104.946$  kcal/mol

deposition (PLD) [58-72] have been reported for depositing  $\text{CeO}_2$  layers on Si (001) and (111) substrates. e-beam evaporation [73-75], sputtering [76-81] and PLD [82-88] have been reported in literature on growth of  $\text{HfO}_2$  layers on silicon. However, a vast majority of recent  $\text{HfO}_2$  research have been performed by using ALD [89-106], as  $\text{HfO}_2$  became the primary choice of semiconductor industry.

Among them, CVD based methods, in particular ALD, are considered to be the industrial choice for deposition of high- $k$  dielectrics because of its precision in layer growth and high layer uniformity in large deposition areas (*i.e.* 300 mm wafer technology). However, ALD has a major disadvantage coming mainly from the long processing time, which makes it an expensive tool to operate. Besides, the demand for complex precursors decreases its flexibility for using in materials research.

Pulsed Laser Deposition (PLD) is known for its flexibility and precision in materials research [26]. High precision layer growth in atomic scale even makes possible to grow artificial materials [107, 108]. High kinetic energy of the ablated material enables low temperature depositions, which is an important feature for growth kinetics. Although PLD is not an industrial option for deposition of high- $k$  gate dielectrics because of its limited layer uniformity in large areas, it's a powerful tool for understanding the properties of high- $k$  oxides, their alloys and structural variations.

#### **1.4. Links Between Electrical and Structural Properties**

Integration of high- $k$  materials to silicon technology needs a deep understanding of their properties. The links between their structural properties (*i.e.* the layer morphology, crystallinity, thermodynamic stability, defects and defect chemistry, interface quality, etc.) and electrical properties (*i.e.* permittivity, charge density, reliability, etc.) have to be established for fulfilling the requirements. Materials and electrical characterization issues of high- $k$  dielectrics have been presented in details in a number of reports [109-119].

In this work, structural characterization of dielectrics grown by pulsed laser deposition are done with X-Ray Photoelectron Spectroscopy (XPS), X-Ray Diffraction (XRD), X-Ray Reflectivity (XRR), Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM) and Atomic Force Microcopy (AFM). Capacitance – Voltage ( $C$ - $V$ ) and Current–Voltage ( $I$ - $V$ ) measurements are used as the electrical characterization tools and the links between electrical and structural properties are tried to be established for binary  $\text{CeO}_2$  and  $\text{HfO}_2$  layers and their laminated structures.

It is aimed to demonstrate the possibilities for improving the electrical properties (EOT and leakage current) of the layers by different deposition approaches,

*i.e.* reducing deposition ambient, lamination of dielectrics *and* using a metal interlayer for interface oxide modifications.

## **1.5. Outline of the Thesis**

The thesis consists of four more chapters: Starting by describing and optimization of the PLD parameters for  $\text{CeO}_2$  and  $\text{HfO}_2$  deposition in Chapter 2 and continuous with the comparison of binary oxides and laminated dielectrics. Chapter 3 includes the details of binary  $\text{CeO}_2$  and  $\text{HfO}_2$  layers deposited as the reference layers for benchmarking the properties of the laminated  $\text{CeO}_2$ - $\text{HfO}_2$  dielectrics, which are presented in Chapter 4. Fabrication of MOSFETs with  $\text{CeO}_2$ - $\text{HfO}_2$  laminated gate dielectrics is presented in Chapter 5.

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# *Chapter 2*

## **Pulsed Laser Deposition of High-*k* Gate Dielectrics**

### **Abstract**

In this chapter, the deposition of high-*k* dielectric layers by PLD is discussed. Basic PLD parameters that affect the layer properties, *i.e.* deposition ambient, deposition temperature, laser fluence, target-to-laser interaction, target-to-substrate distance, are described in detail. Other parameters that directly affect layer properties, like substrate pretreatments and post deposition treatments of dielectric layers, are also discussed.

PLD parameters optimized for growth of CeO<sub>2</sub> and HfO<sub>2</sub> layers are presented. Deposition in reducing ambient followed by *in-situ* oxygen post deposition anneal is proposed for reducing interface oxide thickness.

## 2.1. Introduction

The deposition method of choice has a large impact on the properties of the high- $k$  layers. A number of deposition methods have been presented in literature for high- $k$  dielectrics [1-4]. Each deposition method has its own unique advantages and disadvantages that affect the microstructural and electrical properties of layers, *e.g.* typical deposition temperatures, the chemistry involved, layer uniformity and reproducibility. Pulsed Laser Deposition (PLD) offers a very wide range of deposition parameters, which makes it an attractive tool for investigating the effects of deposition parameters independently.

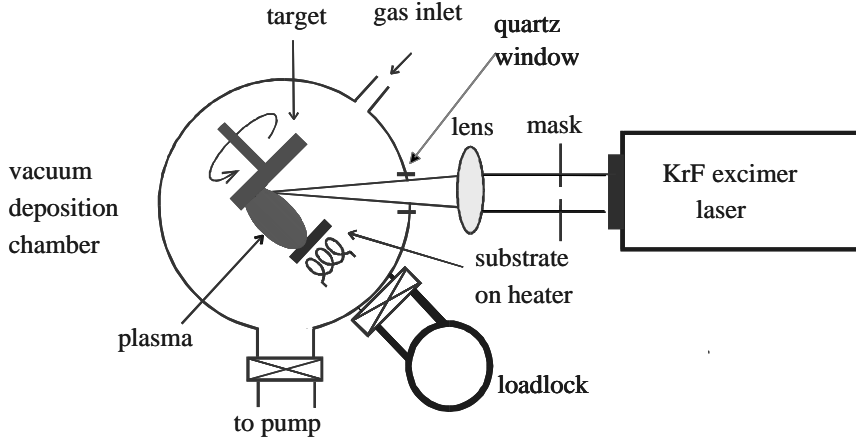
Process steps from substrate preparation to film growth with PLD and post deposition treatments are the major contents of this chapter. Substrate preparation including the native oxide removal from the silicon surface, hydrogen passivation and other surface pretreatments; basic parameters involved in PLD of high- $k$  dielectrics, various process conditions and optimization of PLD parameters are discussed in details.

## 2.2. Pulsed Laser Deposition

PLD is a powerful tool for thin film research. Its flexibility in controlling parameters like deposition temperature, deposition pressure and ambient, target material composition and ablation parameters directly affect plasma formation, film growth and film properties [4, 5]. However, PLD has limited spatial area uniformity, which is defined by process parameters like laser spot size and shape, target-to-substrate distance and deposition pressure [6-8]. Limited spatial area uniformity is obviously a disadvantage of PLD in applications, but on the other hand it can be considered as an advantage for decreasing experimental costs in materials research by means of using smaller substrates compared to the other methods. Typical PLD deposition setup is presented in Figure 2.1. Main advantages of PLD are listed as follows:

- Reduced deposition chamber size by placing the power source outside of the chamber, which eases the pumping operations.
- Ability of using high pressures as well as ultra high vacuum (UHV) conditions.
- Flexibility and good control of substrate temperature by allowing heater designs in different complexity.
- Independent controlling of deposition parameters, like target-to-substrate distance, deposition temperature, deposition pressure, laser fluence.
- High energetic particles in plasma hence increased reactivity by using a large variety of process gases.

- Stoichiometric transfer from target to substrate.
- Multiple target usage for multilayer depositions.
- Highly controllable deposition rates.



**Figure 2.1.:** Schematic view of a PLD setup [4].

Major parameters of PLD and their effects on film properties, physical and chemical processes involved in deposition are described in details in literature [4, 9-22]. In general, parameters which affect properties are summarized as follows:

- Substrate related parameters (substrate properties and pretreatments of substrate).
- PLD parameters (target properties and laser fluency and frequency, laser spot size and shape, target-to-substrate distance, deposition temperature, deposition ambient and pressure).
- Post-deposition treatment (annealing).

In this study a UHV-PLD setup equipped with a high pressure RHEED<sup>1</sup> (Reflection High Energy Electron Diffraction) system [23] is used for deposition of high-*k* layers. Base pressure of the deposition chamber is less than  $5 \cdot 10^{-9}$  mbar and a maximum deposition temperature of 950 °C. The chamber pressure is controlled with a variable valve with a fixed gas flow rate of 30 ml/min<sup>2</sup> and has a scanning target carousel (up to 5 targets)

<sup>1</sup> RHEED is a method uses high energy (10-50 keV) electrons striking the surface at a grazing angle. It gives the information about the periodicity of surface atoms, by the diffraction image formed on properly placed phosphorus screen.

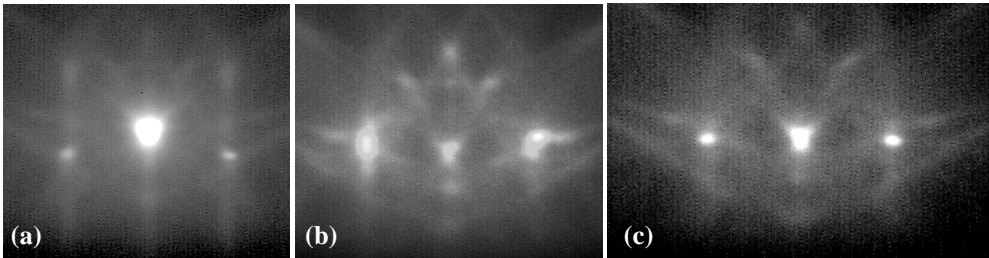
<sup>2</sup> Gas flow rate was fixed at 30 ml/min for this work. The deposition setup has the capability of choosing fixed valve position and changing flow rate for pressure adjustments, as well as choosing another fixed gas flow rate.

## 2.3. Experimental

### 2.3.1. Substrate Preparation

The first step of producing a MOS device with a high-k gate dielectric is the silicon substrate preparation, *i.e.* native oxide ( $\text{SiO}_2$ ) removal and thermal pretreatments like annealing. This step has been reported to be affecting silicon-dielectric interface properties, thin film morphology and electrical properties [24-32].

In this work, native oxide removal of Si (001) substrates is performed by etching with diluted (1%) hydrofluoric acid (HF) solution for 2 min, which results in an oxide free, hydrophobic surface passivated by hydrogen [33-35]. The typical RHEED pattern of HF last<sup>3</sup> Si (001) surfaces is shown in Figure 2.2. Etched Si substrate is loaded to the deposition chamber within 5 minutes. After the chamber is pumped down to  $10^{-7}$  mbar level, it is purged with Ar+H<sub>2</sub> gas mixture (5% H<sub>2</sub>) with a flow rate of 30 l/min for 15 minutes before the substrate temperature is increased. According to the RHEED patterns presented in Figure 2.2, no significant change in surface due to re-oxidation is observed. XPS<sup>4</sup> (X-Ray Photoelectron Spectroscopy) Si 2p spectra of hydrogen passivated surface presented in Figure 2.3 also indicates an oxide free silicon surface after HF etching<sup>5</sup>.



**Figure 2.2:** RHEED pattern of HF etched Si (001) surface. (a) at 20 °C (b) at 600 °C and (c) at 800 °C

Hydrogen on HF etched substrate can be removed by annealing the substrate in the deposition chamber [36]. Annealing of hydrogen passivated silicon surface prior to deposition is reported to improve the gate dielectric and interface morphology [37]. In Figure 2.4, Atomic Force Microscope (AFM) images of two different layers of  $\text{Al}_2\text{O}_3$  (2 nm in thickness) deposited by PLD at room temperature, in vacuum ( $<10^{-7}$  mbar) are

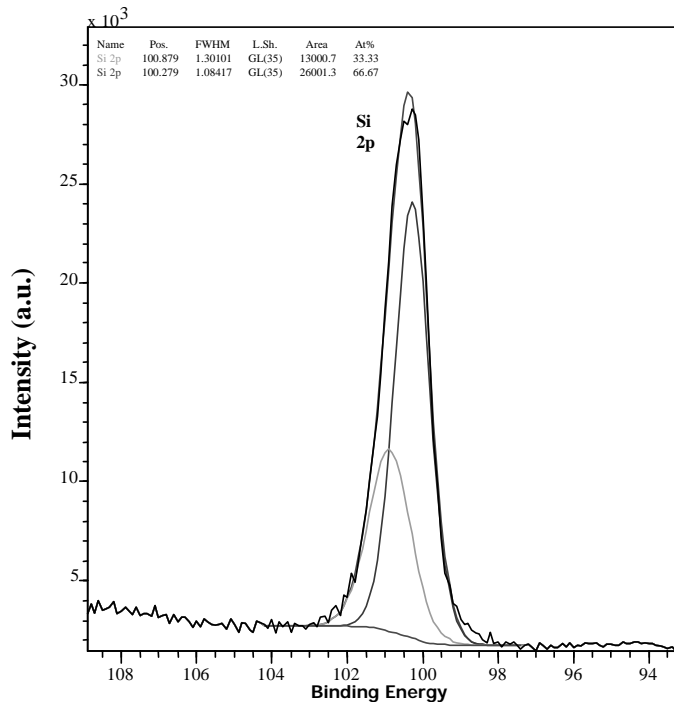
<sup>3</sup> HF etched silicon surface is also called as ‘HF last’, ‘HF dipped’ or ‘H passivated’ in semiconductor science and technology glossary.

<sup>4</sup> XPS is a non-destructive surface sensitive analytical tool which uses X-rays as an excitation source and collects information from the surface elements including their chemical state, which is useful to monitor surface reactions.

<sup>5</sup> HF etched silicon surface is transferred to XPS analysis chamber within 10 minutes after etching, which is the maximum time to delivery of substrate to deposition chamber in this work.

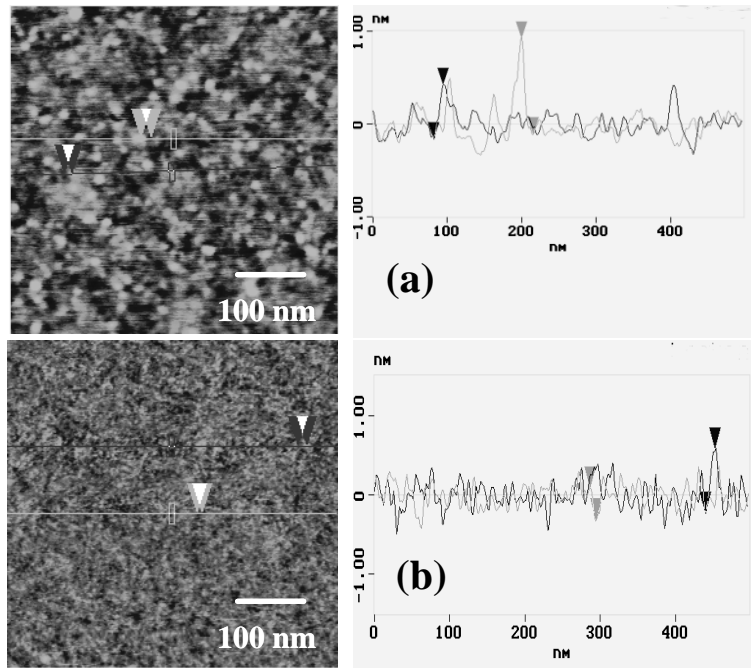


presented. Both substrates are HF etched for native oxide removal and placed into the deposition chamber within 5 minutes after etching. AFM image of the presented in Figure 2.4.a shows the Al<sub>2</sub>O<sub>3</sub> layer deposited at room temperature without annealing in vacuum. The other one, presented in Figure 2.4.b, is first annealed at 500 °C for 15 minutes at 0.1 mbar Ar+H<sub>2</sub> gas mixture, then cooled down to room temperature. The depositions are performed at identical conditions. As can be seen from the figure, annealing the substrate prior to deposition resulted in smoother morphology of deposited Al<sub>2</sub>O<sub>3</sub> layers. Secondary Ion Mass Spectrometry<sup>6</sup> (SIMS) depth profiles of these layers are presented in Figure 2.5, showing the presence of hydrogen (Figure 2.5.a) in the layer deposited on the substrate without annealing *and* no hydrogen is present in the one deposited after substrate annealing (Figure 2.5.b)

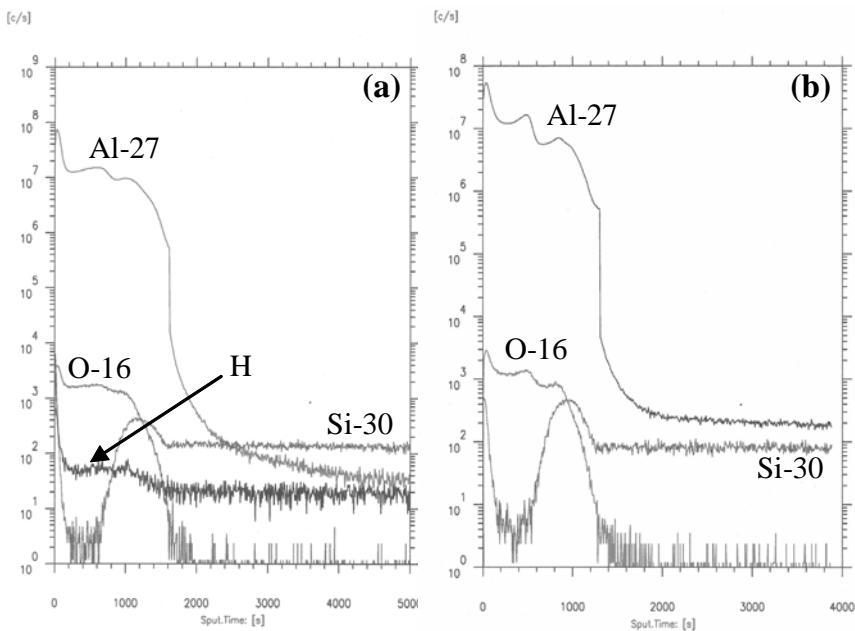


**Figure 2.3:** XPS spectra of Si 2p peak of HF etched silicon substrate. The inner curves are the fits for the experimental curve placed outermost of the graph.

<sup>6</sup> SIMS is a surface analysis tool based on mass spectrometry by analyzing the secondary ions produced during sputtering by a high energy ion beam. In this analysis, a Cameca IMS-6f tool with Cs<sup>+</sup> ion gun is used.



**Figure 2.4:** AFM images of room temperature deposited 2 nm thickness  $\text{Al}_2\text{O}_3$  layers on silicon (image size is  $500 \times 500 \text{ nm}^2$  and depth scale is 4 nm) (a) deposition on HF last surface (b) after annealing at  $500^\circ\text{C}$  in  $\text{Ar}+\text{H}_2$  for 15 min.



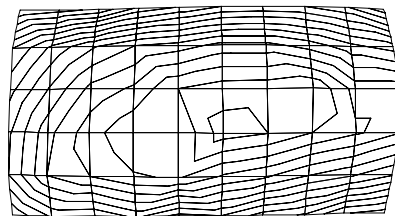
**Figure 2.5:** SIMS depth profiles of 2 nm  $\text{Al}_2\text{O}_3$  layers grown by PLD at room temperature on substrates without annealing (a), and after annealing at 0.1 mbar (30 l/min)  $\text{Ar}+\text{H}_2$  gas mixture  $500^\circ\text{C}$  for 15 minutes and cooled down to room temperature (b).

Another critical step in PLD is the preablation<sup>7</sup> of targets prior to deposition. This step is performed to clean the target surface by means of removing the contaminants on the surface by ablation, and more importantly, for achieving a stable surface morphology and homogenous chemical composition on surface [38, 39]. It has been shown that the preablation of targets increases oxygen potential in the deposition chamber and causes oxidation of silicon surfaces [40]. Therefore, in this study, preablation is always performed before loading the substrate into deposition chamber in order to prevent oxidation of silicon surface before deposition.

### 2.3.2. Pulsed Laser Deposition Parameters

Optimization of the PLD parameters starts with determining the best laser energy density by monitoring the laser-target interaction. The energy density of the laser beam, for a given pulse duration and pulse frequency, changes the morphological and compositional stability of target surface during deposition process [38]. Although the compositional change of the surface during ablation is not considered to be a problem for binary oxides, rough target surfaces during ablation may cause inhomogeneous ablation, and may result in problems like particulate ejection from target surface during deposition.

A KrF (248 nm wavelength) pulsed laser<sup>8</sup>, with a pulse duration of 20 ns (FWHM), is used in this work. The energy profile of the used laser beam is given in Figure 2.6. Laser light is driven to the deposition chamber by a beam guide, consisting of beam rotators and mirrors directing the beam to the chamber. An aluminum mask, which filters the homogenous energy density part of the beam, also defines the laser spot size and shape. A lens for focusing the beam on to the target is placed in front of the laser entrance window with a known laser transmittance. The laser beam entered the deposition chamber at an angle of 45° to the target normal. Energy measurements of the laser beam are performed after the lens in order to minimize the measurement errors originated by the loss caused by mirrors in the beam path.



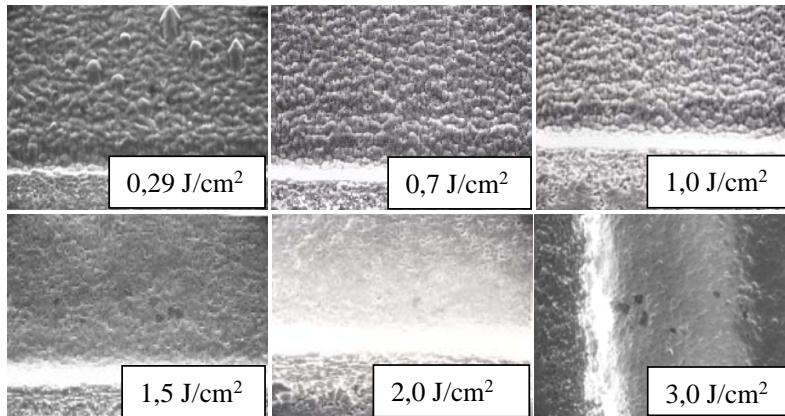
**Figure 2.6:** Laser beam energy profile contour of the laser used in this work in 18 x 10 mm<sup>2</sup> area. The central area of the graph shows 4.5-4.6 mJ, outermost region is 3.6 mJ and each line represents 0.1 mJ range.

<sup>7</sup> Typically, a shutter is placed in front of the substrate to prevent deposition during preablation.

<sup>8</sup> LPX 200 Lambda Physik laser source is used in this work.

Figure 2.7 shows the surface morphology of the  $\text{Al}_2\text{O}_3$  target after 500 laser pulses at 5 Hz at different laser fluencies. As can be seen from these Scanning Electron Microscope (SEM) micrographs, target surface morphology depends on the laser energy density starting from  $0.29 \text{ J/cm}^2$ , which is close to the ablation threshold of  $0.25 \text{ J/cm}^2$  for the  $\text{Al}_2\text{O}_3$  target, going to  $3 \text{ J/cm}^2$ . Smoothest layers are achieved with a  $3 \text{ J/cm}^2$  energy density and this is chosen as the energy density for deposition.

The same procedure is applied for  $\text{CeO}_2$  and  $\text{HfO}_2$  targets to optimize the energy density for a particulate free deposition.  $1$  and  $3 \text{ J/cm}^2$  was found as the optimum energy density for  $\text{CeO}_2$  and  $\text{HfO}_2$  targets, respectively. Figure 2.8 shows the AFM images of room temperature deposited  $\text{CeO}_2$  layers deposited on hydrogen passivated silicon at room temperature,  $0.1 \text{ mbar Ar+H}_2$  and a target-to-substrate distance of  $45 \text{ mm}$ , with  $0.5$ ,  $1$  and  $1.5 \text{ J/cm}^2$  energy densities. According to the AFM images,  $1 \text{ J/cm}^2$  gives the smoothest layers and confirms the optimized  $\text{CeO}_2$  target ablation parameters for this deposition conditions.

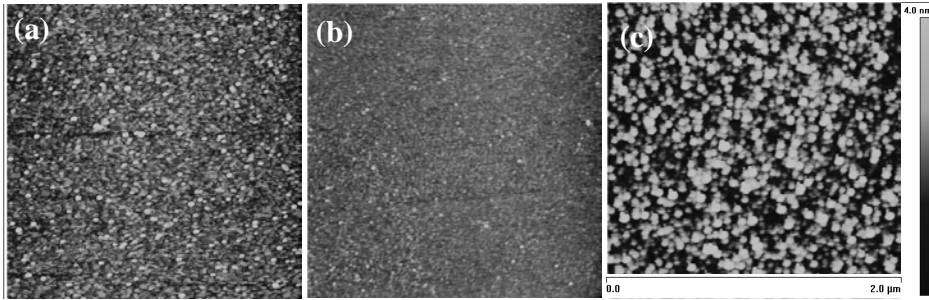


**Figure 2.7:**  $\text{Al}_2\text{O}_3$  target surface morphology after 500 laser pulses at 5 Hz with different energy densities.

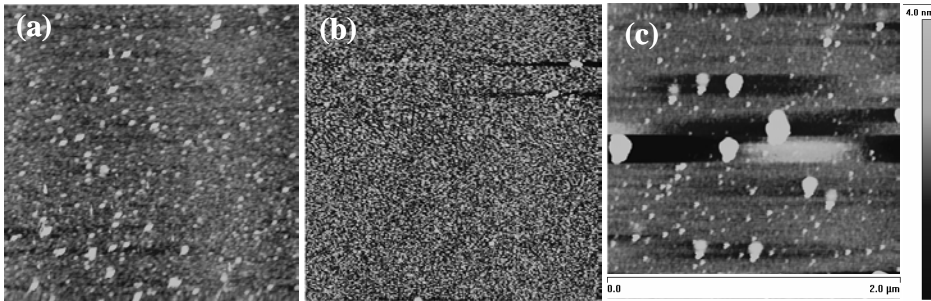
$\text{HfO}_2$  layers grown at identical conditions as in the  $\text{CeO}_2$  depositions, except the energy densities, are presented in Figure 2.9.  $\text{HfO}_2$  layers are deposited at  $1.5$ ,  $3$  and  $3.5 \text{ J/cm}^2$ , and  $3 \text{ J/cm}^2$  is chosen as the optimum energy density for  $\text{HfO}_2$  depositions, as it gave the smoothest layer, as expected by target morphology observations, which showed a steady surface morphology at  $3 \text{ J/cm}^2$ .

Plasma dynamics in PLD are directly related with the deposition pressure and ambient. Presence of an ambient gas increases the number of collisions with ablated species and results in confinement in plasma. As a rule of thumb, the drag force model for low pressures (up to  $0.1 \text{ mbar}$ ) and shock wave model for higher ambient pressures are used to explain plasma expansion dynamics [4]. In this work, ambient pressure of  $0.1 \text{ mbar}$  is chosen as fixed ambient pressure independent from the gas type (Ar,

Ar+5% $H_2$  mixture or  $O_2$ ) and target-to-substrate distance of 45 mm is set to place the substrate holder to the plasma edge.



**Figure 2.8:** AFM images of  $CeO_2$  layers deposited on hydrogen passivated silicon at room temperature, at 0.1 mbar  $Ar+H_2$  by three different laser energy densities of  $0.5 J/cm^2$  (a),  $1 J/cm^2$  (b), and  $1.5 J/cm^2$  (c). Image size is  $2 \times 2 \mu m^2$  with a depth scale of 4 nm.



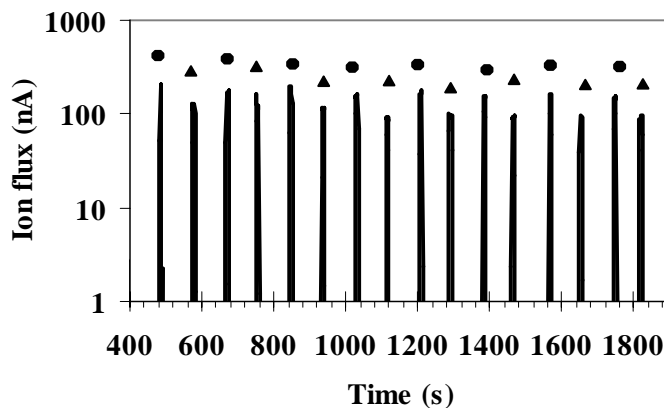
**Figure 2.9:** AFM images of  $HfO_2$  layers deposited on hydrogen passivated silicon at room temperature, at 0.1 mbar  $Ar+H_2$  by three different laser energy densities of  $1.5 J/cm^2$  (a),  $3 J/cm^2$  (b), and  $3.5 J/cm^2$  (c). Image size is  $2 \times 2 \mu m^2$  with a depth scale of 4 nm.

The majority of this thesis is based on laminated dielectrics made of alternating layers of  $CeO_2$  and  $HfO_2$ , which are deposited sequentially. When depositing several types of oxides in one deposition run, changing the laser beam energy by changing the laser source operating parameters is not an efficient way because of causing energy instabilities after each change. Instead, using proper masks with different areas and aligning the optics accordingly, enables changing the energy density on the target without manipulating the laser source parameters. In order to maintain the selected energy densities on the targets and a deposition rate which allows precise controlling of the layer thicknesses of individual layers in laminated structures, two different masks are used, which are changed properly before deposition of different oxides. By using these settings, a  $0.025 \text{ nm/pulse}$  deposition rate is achieved for both  $CeO_2$  and  $HfO_2$ . Table 2.1 summarizes the deposition parameters used in this work, for  $CeO_2$  and  $HfO_2$  deposition by PLD.

**Table 2.1:** PLD parameters for CeO<sub>2</sub> and HfO<sub>2</sub> thin film growth.

	CeO <sub>2</sub>	HfO <sub>2</sub>
Ambient pressure	0.1 mbar	0.1 mbar
Energy density	1 J/cm <sup>2</sup>	3 J/cm <sup>2</sup>
Laser pulse frequency	5 Hz	5 Hz
Target to substrate distance	45 mm	45 mm
Deposition rate	0.025 nm/pulse	0.025 nm/pulse

At the deposition conditions described above, the ionic fluxes of CeO<sub>2</sub> and HfO<sub>2</sub> plasmas in 0.1 mbar Ar+H<sub>2</sub>, measured by an ion probe placed to the side of the plasma during ablation are presented in Figure 2.10. Each peak corresponds to 1 nm (approximately) oxide deposition. After ablation of one oxide, the target carousel is rotated for the other oxide, laser mask has changed and then the ablation started. This procedure is repeated to complete laminated structures. Note that the probe is not placed to the plasma front, where the substrate is placed and the measured ion fluxes are presented only for showing the consistency after each target change.



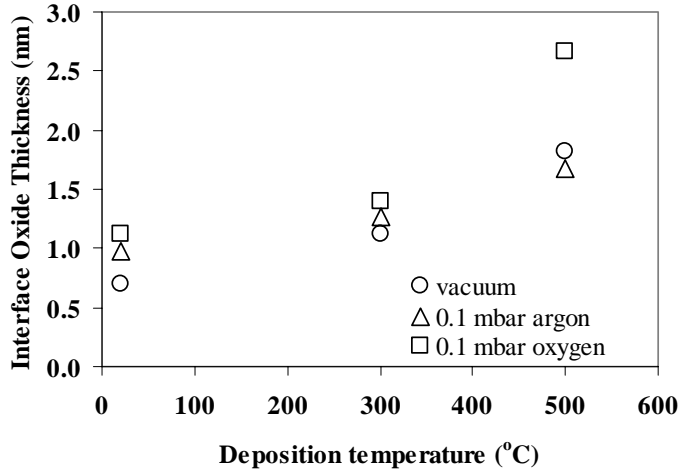
**Figure 2.10:** Measured ion fluxes of CeO<sub>2</sub> (circles) and HfO<sub>2</sub> (triangles) in 16 nm laminated CeO<sub>2</sub>-HfO<sub>2</sub> dielectric deposition. Each peak corresponds to 40 laser pulses at 5 Hz with 1 and 3 J/cm<sup>2</sup> energy densities on CeO<sub>2</sub> and HfO<sub>2</sub> targets respectively.

### 2.3.3. Deposition of CeO<sub>2</sub> Layers

First runs for CeO<sub>2</sub> layers by PLD, were performed for understanding the effect of basic deposition parameters, like deposition temperature and ambient, on interfacial oxide thickness in particular and film morphology.

Figure 2.11 shows the dependency of interface oxide thickness of CeO<sub>2</sub> layers on deposition ambient and temperature. The layers are deposited at vacuum ( $<10^{-7}$

mbar), argon (0.1 mbar) and oxygen (0.1 mbar) at three different deposition temperatures of room temperature, 300 and 500 °C. The interface oxide thickness is based on simulations of Rutherford Backscattering<sup>9</sup> (RBS) analysis. According to the analyses, interface oxide thicknesses of the layers deposited in O<sub>2</sub> are larger than the ones deposited in vacuum (<10<sup>-6</sup> mbar) or Ar.



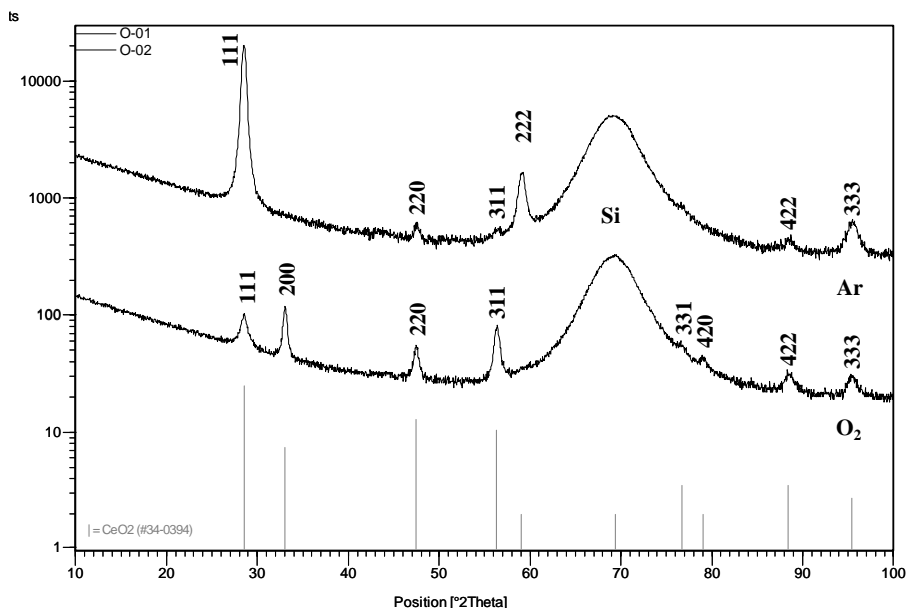
**Figure 2.11:** Interface oxide thickness of CeO<sub>2</sub> layers grown on hydrogen passivated Si (001) in different deposition ambient and temperature.

As a second step, effects of deposition ambient on the CeO<sub>2</sub> layer structure are investigated. Layers deposited at 800 °C in oxygen and argon, on Si (001) with a chemically grown SiO<sub>2</sub> on top, were analyzed by X-Ray Diffraction<sup>10</sup> (XRD) and X-Ray Reflection (XRR) measurements. According to the XRD scan (Figure 2.12), CeO<sub>2</sub> layer grown in Ar shows a preferred orientation on (111) direction, where the one grown in O<sub>2</sub> shows a random orientation as all the peaks for cubic (fluorite) CeO<sub>2</sub> are present with comparable intensities. The wide peak located around 69° belongs to silicon substrate. XRR data of the layers are presented in Figure 2.13, which shows the presence of second series of fringes with much larger wavelength<sup>11</sup> than the fringes of CeO<sub>2</sub> layer for the one deposited in Ar. This indicates the presence of a second layer with a different electron density.

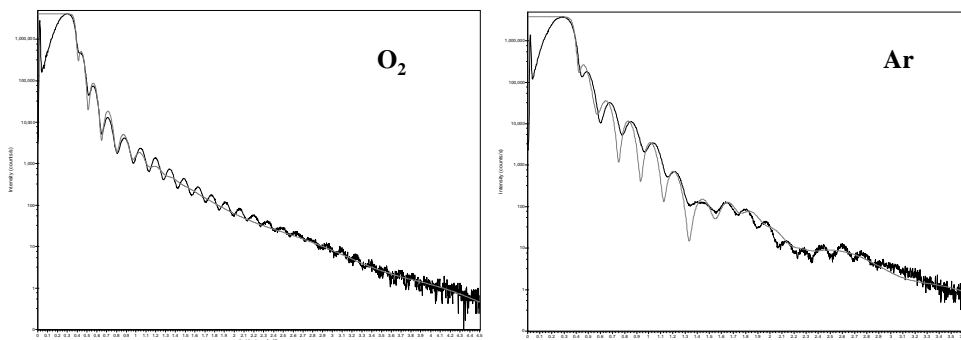
<sup>9</sup> RBS is an analytical tool which uses accelerated He<sup>+</sup> ions and collects information from analyzed surface by means of comparing the energies of backscattered ions. The technique, in principle, doesn't give the information about interfacial oxide thickness but by keeping the simulation parameters the same; one can compare the results for interface oxide thicknesses for different deposition conditions.

<sup>10</sup> XRD measurements have been performed with a Philips PW1800 diffractometer, equipped with a Cu anode and a graphite monochromator in the diffracted beam to select only the Cu K $\alpha$  radiation.

<sup>11</sup> Term 'wavelength' is used for indicating the periodicity of the fringes in XRR analysis regarding to the simulations.



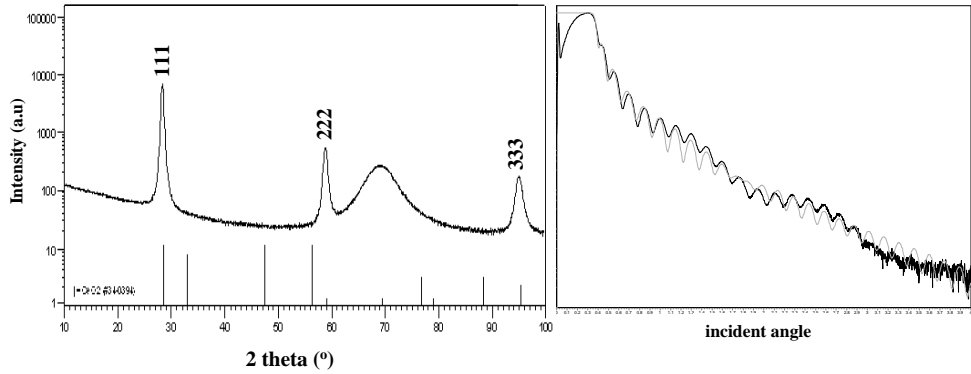
**Figure 2.12:** XRD  $2\theta$  scan of  $\text{CeO}_2$  layers grown on Si (001), with a chemically grown  $\text{SiO}_2$  layer on top, deposited at  $800^\circ\text{C}$  in 0.1 mbar  $\text{O}_2$  and Ar.



**Figure 2.13:** XRR scan of the  $\text{CeO}_2$  layers grown in 0.1 mbar  $\text{O}_2$  (left) and Ar (right) ambient at  $800^\circ\text{C}$  on Si (001) with a chemically grown  $\text{SiO}_2$  layer on top. The thicknesses from the XRR simulations are 24.7 nm for the layer deposited in  $\text{O}_2$  and 20.6 nm for the layer deposited in Ar.

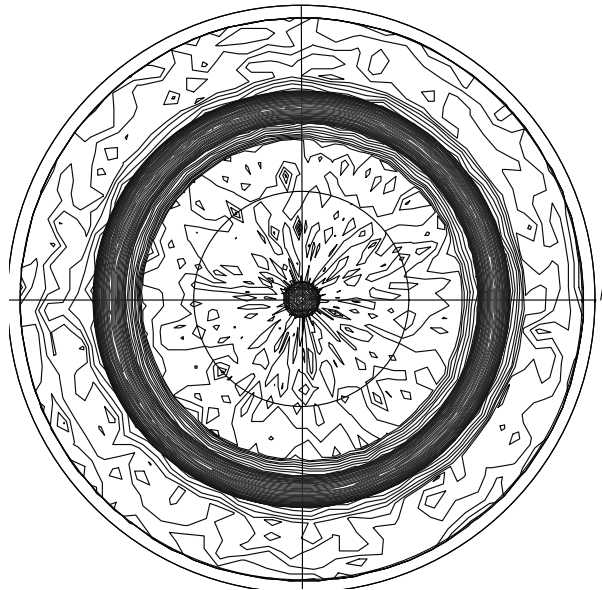
In order to confirm that the presence of the second layer is not related with the chemically grown  $\text{SiO}_2$  layer on top of Si (001) substrate, another  $\text{CeO}_2$  layer is deposited on hydrogen passivated Si (001) in Ar. The XRD pattern (Figure 2.14, left) shows the preferred orientation of  $\text{CeO}_2$  layer in (111) direction similar to the layer grown in Ar presented in Figure 2.12. The XRR analysis of this layer (in Figure 2.14, right), is also found to be similar to the layer deposited in Ar on Si (001) with a chemically grown  $\text{SiO}_2$  layer on top.





**Figure 2.14:** XRD  $2\theta$  scan (left) and XRR analysis (right) of  $\text{CeO}_2$  layer grown on hydrogen passivated Si (001), deposited at  $800^\circ\text{C}$  in Ar. Layer thickness is 26.5 nm according to the XRR simulation.

For better understanding the nature of orientation of  $\text{CeO}_2$  layers grown in Ar ambient, pole figure analysis of the layer deposited in Ar ambient on hydrogen passivated Si (001) was performed (Figure 2.15). Data were recorded at  $2\theta=33.14^\circ$  (the (200) peak of  $\text{CeO}_2$ ), which does not overlap with a Si peak) tilting the sample from  $\Psi=0^\circ$  to  $85^\circ$  and rotating it from  $\phi=0^\circ$  to  $360^\circ$  both with a step size of  $5^\circ$ , such that most orientations of the sample in space have been covered. Ring shaped pole figure indicates that crystallites have all possible orientations around an axis perpendicular to the surface.



**Figure 2.15:** Pole figure along the (002) peak of  $\text{CeO}_2$  layer grown in 0.1 mbar Ar at  $800^\circ\text{C}$ . Ring shaped pattern indicates the layer have a preferred orientation along (111) direction.

Dependency of PLD grown CeO<sub>2</sub> layers on deposition ambient has been reported in literature [41-43]. In these reports, orientation of CeO<sub>2</sub> layers is related to the oxygen pressure during deposition: As the oxygen pressure increases, layers tend to orientate in (001) instead of (111) direction. It has been reported that the oxygen deficient interfacial layers formed by the reaction of oxide with silicon, may cause this ambient dependency in orientation [42].

According to the simulations based on XRR analysis (shown in Figure 2.13 and 2.14) the secondary layer formed between the SiO<sub>x</sub> and CeO<sub>2</sub> layers, was found to be between 3-5 nm in thickness. A good explanation of an oxygen deficient layer formation in cerium oxide layers on silicon, comes from the chemical reactivity of ablated species of CeO<sub>2</sub> ablation in PLD [44-47]: During pulsed laser ablation of CeO<sub>2</sub>, negative (CeO<sup>-</sup>, CeO<sub>2</sub><sup>-</sup>, CeO<sub>3</sub><sup>-</sup>, CeO<sub>4</sub><sup>-</sup>) and positive (Ce<sup>+</sup>, CeO<sup>+</sup>, Ce<sub>2</sub>O<sub>3</sub><sup>+</sup>, Ce<sub>3</sub>O<sub>4</sub><sup>+</sup>, Ce<sub>3</sub>O<sub>5</sub><sup>+</sup>) ions and clusters ([Ce(CeO<sub>2</sub>)<sub>n</sub>]<sup>+</sup>, [CeO(CeO<sub>2</sub>)<sub>n</sub>]<sup>+</sup>, n<sub>max</sub>=3) are formed in the ablation plume according to mass spectrometry analysis. Presence of these ions and clusters in the plume in a non-oxidizing ambient, may lead oxygen deficient layers.

Thermodynamic calculations based on vapor pressure, in equilibrium with the solid or the liquid target of CeO<sub>2</sub>, has been showed a phase transition on target surface from CeO<sub>2</sub> to Ce<sub>2</sub>O<sub>3</sub> gradually *and* it also has been showed that at temperatures above 3000 K Ce<sub>2</sub>O<sub>3</sub> becomes the dominant phase [46]. In the same work, layers deposited at different oxygen pressures analyzed by XPS and it's found that Ce (III) (presence of reduced species as Ce<sub>2</sub>O<sub>3</sub>) is more dominant than Ce (IV) (CeO<sub>2</sub>) in the deposited layers. Oxygen loss in CeO<sub>2</sub> films grown by PLD has been reported as well, and it's correlated to UV-laser irradiation during deposition [45].

Deposition in reducing ambient, with presence of hydrogen<sup>12</sup> is likely to have an increasing effect on Ce<sub>2</sub>O<sub>3</sub> formation in the deposited layer. As mentioned in Chapter 1, Ce<sub>2</sub>O<sub>3</sub> is more stable than CeO<sub>2</sub> on silicon for interface oxide formation reaction<sup>13</sup> [48]. In other terms, Ce<sub>2</sub>O<sub>3</sub> formation during deposition can be preferable in terms of limitation of interface oxide formation. Therefore, a new deposition approach is shaped based on that idea of using a reducing ambient during deposition of dielectrics, which is discussed in details in the next section of this chapter.

### 2.3.4. Reducing Ambient Deposition

Reducing ambient during deposition is achieved by a gas mixture of Ar and 5% H<sub>2</sub>. Effect of hydrogen is a critical issue in silicon technology and in general, is divided

<sup>12</sup> Molecular hydrogen thermally decomposes to atomic hydrogen around 3000 K, which is in range of plasma temperature in ablated plume.

<sup>13</sup> CeO<sub>2</sub>:  $\Delta G_{1000}=+36.290$  kcal/mol - Ce<sub>2</sub>O<sub>3</sub>:  $\Delta G_{1000}=+104.946$  kcal/mol for interface oxide formation reaction on silicon:  $Si + MO_x \rightarrow SiO_2 + M$

into two sub discussions: Effect of hydrogen at silicon-dielectric interface *and* in dielectric thin film.

Forming gas (a gas mixture of 5-10% H<sub>2</sub> with N<sub>2</sub>) annealing at temperatures around 400 °C, to passivate the interface states at the Si-SiO<sub>2</sub> interface, is a usual process step in semiconductor technology. It was early recognized as an effective way of increasing device performances. But in later years, depassivation of interface traps by a reverse process, in particular in irradiated MOS systems has been noticed [49]. Depassivation of interface states by release of hydrogen has also been correlated to the electric field stress in MOS structures, which causes negative bias temperature instability (NBTI) [50-54].

Hydrogen in the oxide layer can originate from deposition processes<sup>14</sup> or from forming gas anneal. Hydrogen release by hole injection in thermally grown SiO<sub>2</sub> layers [51, 53, and 55] and effects in high-*k* dielectrics has been reported in literature and possible mechanisms are discussed [50, 51, 54, 56-58]. Since NBTI is not studied in this work, it's not possible to draw a conclusion on the effect of hydrogen in CeO<sub>2</sub>-HfO<sub>2</sub> layers grown by PLD.

Another major concern with respect to the reducing ambient deposition is the creation of oxygen vacancies in the dielectric layer. This causes instabilities in electrical properties of devices [59, 60]. Therefore PLD in reducing ambient of dielectrics should include an oxidizing post deposition anneal (PDA). In this work, an *in-situ* PDA in high oxygen pressure (p<sub>O<sub>2</sub></sub>=100 mbar) is applied during cooling down of the layers from deposition temperature to room temperature, which has not been reported previously in the literature about reducing ambient PLD of CeO<sub>2</sub> thin films [43, 61].

*In-situ* PDA after deposition is performed as follows:

- Chamber is pumped down for removing deposition gas (Ar+H<sub>2</sub>) to 10<sup>-6</sup> mbar level (~2-3 minutes).
- Oxygen (p<sub>O<sub>2</sub></sub>=100 mbar<sup>15</sup>) introduced to the chamber.
- Substrate is cooled down to room temperature with a given cooling rate<sup>16</sup>.

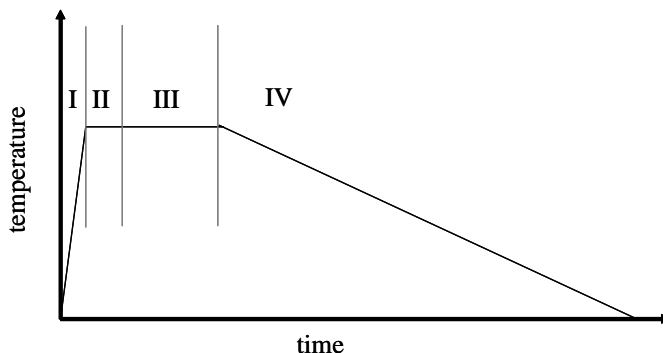
A typical thermal cycle in reducing ambient PLD followed by *in-situ* PDA is presented in Figure 2.16. After loading the substrate, the chamber is pumped down to 10<sup>-8</sup> mbar, and then purged with 30 l/min Ar+H<sub>2</sub> gas flow (p=0.1 mbar) for 15 minutes

<sup>14</sup> Besides the reducing ambient deposition as performed in this work, other deposition methods like ALCVD, involves water and organo-metallic precursors during deposition which also causes hydrogen 'contamination' in the layers.

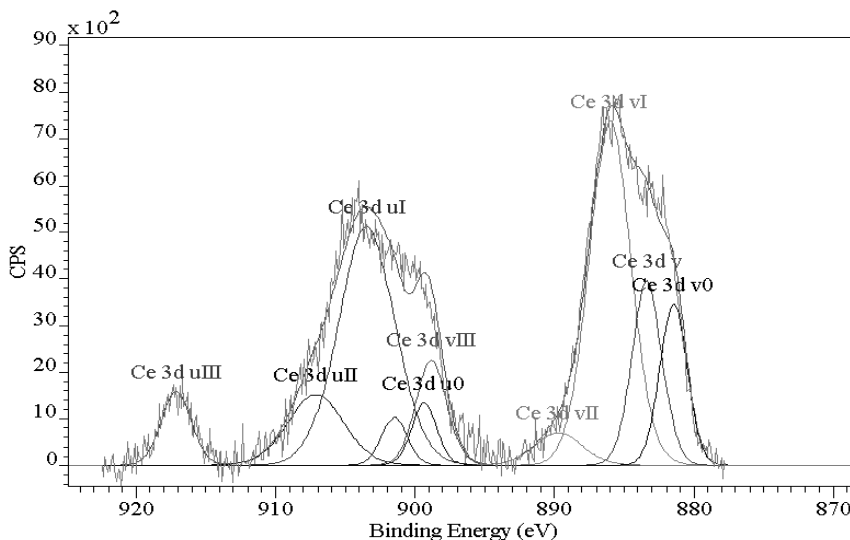
<sup>15</sup> 100 mbar is set as the standard pressure for PDA but the deposition system was not optimized to operate at high pressures. It was not possible to control the PDA pressure as precise as in deposition pressure regime. The pressure during PDA should be considered in error range of ±10 mbar.

<sup>16</sup> 5 °C/min is used as standard cooling rate in this work. 2 and 10 °C/min cooling rates are also used in order to monitor the effect of oxidation kinetics during PDA.

before heating up the substrate to deposition temperature (step I). Substrate is annealed for 15 minutes (step II) in 0.1 mbar Ar+H<sub>2</sub> and then the deposition started (step III). PDA is then performed in the routine as described above.



**Figure 2.16:** Typical thermal cycle in reducing ambient deposition followed by PDA: I: heating up substrate to deposition temperature. II: annealing of substrate (15 minutes). III: PLD and IV: *in-situ* PDA. Steps I, II and III are carried out in 0.1 mbar Ar+H<sub>2</sub>, step IV is in 100 mbar O<sub>2</sub>. Note that the graph is not scaled neither to temperature, nor the time.

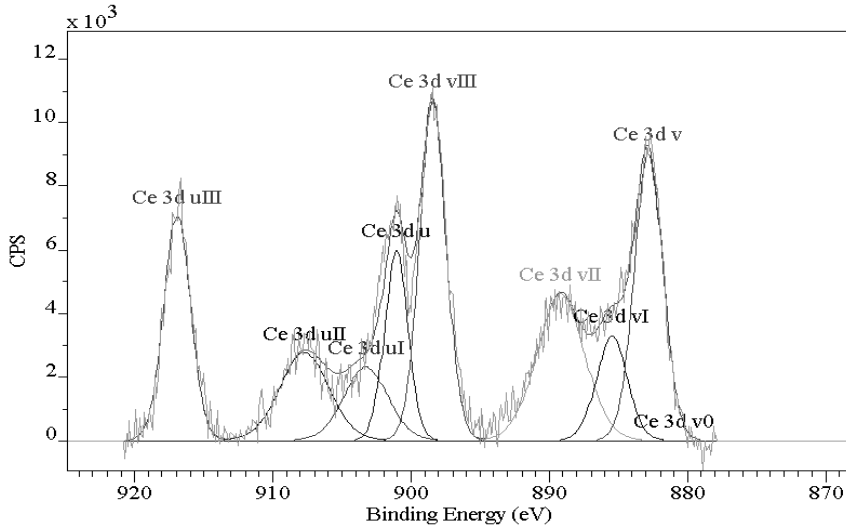


**Figure 2.17:** Ce XPS spectra of the 2 nm CeO<sub>2</sub> layer deposited in reducing ambient, without oxidizing with *in-situ* PDA.

The effect of *in-situ* PDA on oxidation of reducing ambient PLD grown CeO<sub>2</sub> layers was investigated by XPS<sup>17</sup>. Figure 2.17 shows the Ce XPS spectra of 2 nm CeO<sub>2</sub> layer deposited in 0.1 mbar Ar+H<sub>2</sub> at 420°C without *in-situ* PDA, as Figure 2.18 shows the one deposited in identical conditions and oxidized with *in-situ* PDA. According to

<sup>17</sup> An angle resolved XPS is used in this work with a limited sputtering capability. Therefore majority of XPS analysis is performed without sputtering, if otherwise is not indicated.

the difference between the two XPS spectra, *in-situ* PDA after deposition provides a highly oxidized CeO<sub>2</sub> layer (Ce III is almost not visible). The layer without PDA shows a significant amount of Ce III, which indicates the presence of Ce<sub>2</sub>O<sub>3</sub> in the layer as the major compound.



**Figure 2.18:** Ce XPS spectra of the 2 nm CeO<sub>2</sub> layer deposited in reducing ambient, after oxidizing with *in-situ* PDA.

An important aspect of the post deposition anneal is its dependency on the layer thickness and the deposition temperature. Diffusion of oxygen during annealing is directly related to the annealing temperature and increases by the increased deposition temperature and the decreasing cooling rate. For a given deposition temperature and a cooling rate, diffusion of oxygen for oxidizing the layers is limited. Besides oxidizing the layers, oxygen diffusion to the interface may result in an increase in interface oxide (SiO<sub>2</sub>) thickness. Therefore fine tuning of *in-situ* PDA for a given layer thickness and deposition temperature is required for limiting interface oxide thickness, or at least for limiting the excessive increase in interface oxide thickness.

## 2.4. Conclusions

Major parameters of the PLD regarding deposition of high-*k* dielectrics, in particular CeO<sub>2</sub> and HfO<sub>2</sub>, are presented in this chapter. Starting from the substrate preparation to the post deposition treatments, major points and conclusions about PLD of high-*k* dielectrics can be listed as follows:

- Native oxide removal from Si surface is performed by HF etching. No oxidation is observed on HF etched substrates during the time to transfer to the deposition chamber.
- Annealing the substrate prior to the deposition is found to be improving the deposited layer quality. SIMS analysis of Al<sub>2</sub>O<sub>3</sub> layers grown at room temperature on annealed and not annealed substrates showed that hydrogen is present in the layer grown on not annealed substrate, whereas the layer grown on annealed substrate didn't have hydrogen. However, it's not clear that the change in layer morphology is directly related to hydrogen desorption. A possible surface reconstruction during annealing may also lead such result.
- PLD parameters are optimized for low deposition rate in order to get a better control on the individual layer thicknesses in laminated dielectrics. A deposition rate of a 0.025 nm/pulse is achieved for both, CeO<sub>2</sub> and HfO<sub>2</sub> layers by using the optimized PLD parameters
- It's been showed that, deposition ambient has a strong effect on CeO<sub>2</sub> layer texture and the layers grown in Ar showed preferred orientation in (111) direction, where as the layers deposited in O<sub>2</sub> have a random orientation. It's also found that the CeO<sub>2</sub> films grown in argon have a secondary layer between CeO<sub>2</sub> and interface oxide (SiO<sub>x</sub>) layers. As supported by the literature, it's concluded as an oxygen deficient layer, *i.e.* Ce<sub>2</sub>O<sub>3</sub>. This conclusion led the studies to reducing ambient deposition for getting the benefit of higher thermodynamical stability of Ce<sub>2</sub>O<sub>3</sub> than CeO<sub>2</sub> on silicon. Therefore, deposition in reducing ambient, by using a gas mixture of Ar+5%H<sub>2</sub> is proposed.
- An in-situ post deposition anneal at high pressure (~100 mbar) oxygen is used for oxidizing the layers deposited in Ar+H<sub>2</sub>. Efficiency of *in-situ* PDA for oxidizing the layers is shown for 2 nm CeO<sub>2</sub> layer deposited at 420 °C in Ar+H<sub>2</sub>.

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# *Chapter 3*

## **CeO<sub>2</sub> and HfO<sub>2</sub> Binary Oxides as High-*k* Gate Dielectrics**

### **Abstract**

CeO<sub>2</sub> and HfO<sub>2</sub> layers are prepared by pulsed laser deposition in reducing ambient, followed by an in-situ oxidizing post deposition anneal. Electrical characterization is done by MOS structures with TaN electrodes and their structural properties are characterized by TEM and XRD analyses. Properties of the layers are used as a reference data for benchmarking the quality of CeO<sub>2</sub>-HfO<sub>2</sub> laminated structures.

### 3.1. Introduction

As it is aimed in this study, for comparing the properties of the binary oxides<sup>1</sup> with their laminated structures, CeO<sub>2</sub> and HfO<sub>2</sub> layers are deposited on Si (001) substrates as reference layers for benchmarking the CeO<sub>2</sub>-HfO<sub>2</sub> laminated structures<sup>2</sup>.

In literature, pulsed laser deposition (PLD) of CeO<sub>2</sub> [1-15] and HfO<sub>2</sub> [16-22] layers on silicon (001) and (111) substrates has been reported. As described in Chapter 2, reducing ambient deposition of these oxides, followed by an *in-situ* oxidizing post deposition anneal (PDA) is performed for investigating the possible improvements in the layer's properties, in particular the interface oxide thickness reduction.

In this chapter, properties of the CeO<sub>2</sub> and HfO<sub>2</sub> layers, with a thickness range of 4 to 16 nm are presented. Their structural characterization is performed by atomic force microscope (AFM), X-Ray diffraction (XRD) and transmission electron microscope (TEM) analyses *and* electrical properties are characterized by capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements.

### 3.2. Experimental

CeO<sub>2</sub> and HfO<sub>2</sub> are deposited at 420 °C and 520 °C as reference layers for further comparison of the properties of the CeO<sub>2</sub>-HfO<sub>2</sub> laminated dielectrics. The thicknesses of the layers were 4, 8, 12 and 16 nm. Layers were deposited in 0.1 mbar Ar+H<sub>2</sub> from CeO<sub>2</sub> and HfO<sub>2</sub> targets, with an energy density of 1 and 3 J/cm<sup>2</sup>, respectively. Target to substrate distance was 45 mm during deposition. An *in-situ* oxidizing PDA is performed in 100 mbar O<sub>2</sub>, with a cooling rate of a 5 °C/min from deposition temperature to room temperature. MOS devices with the layers are produced by using TaN electrodes<sup>3</sup>, which were prepared by *ex-situ* sputtering at room temperature, followed by a plasma etching step for patterning. Electrical measurements (*C-V* and *I-V*) are performed at room temperature.

### 3.3. Results and Discussion

In this section, the structural and electrical properties of the CeO<sub>2</sub> and HfO<sub>2</sub> layers are presented separately.

#### *Structural Characterization*

AFM images of CeO<sub>2</sub> reference layers in various thicknesses deposited at 420 and 520 °C are presented in Figure 3.1. No major differences are observed for the

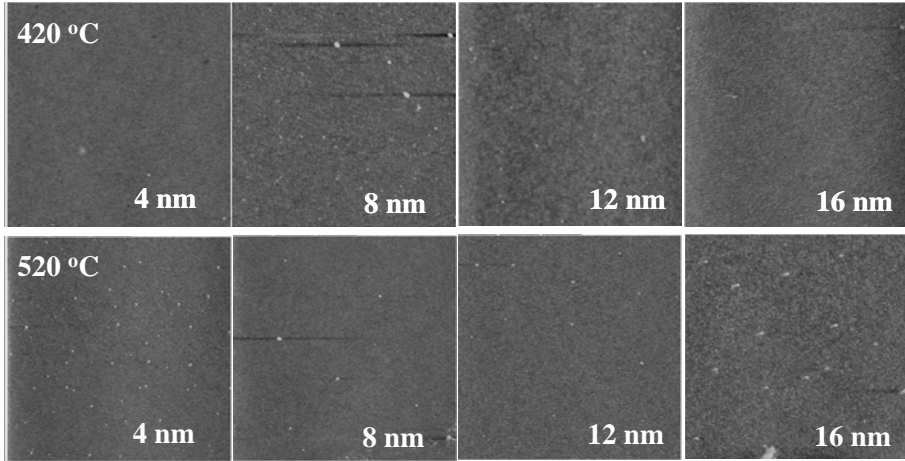
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<sup>1</sup> The binary oxide term is the typical notation for describing the oxides with two elements; a metal and oxygen (MO<sub>x</sub>).

<sup>2</sup> CeO<sub>2</sub>-HfO<sub>2</sub> laminates are presented in Chapter 4.

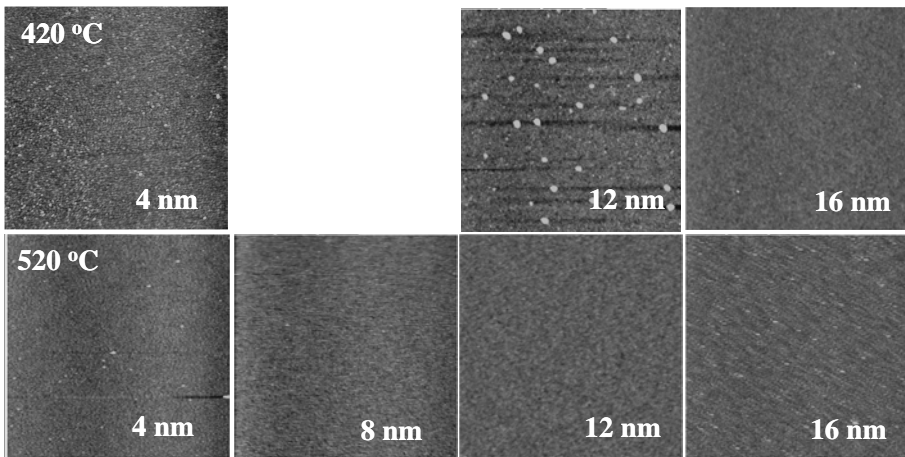
<sup>3</sup> Details of TaN electrode processing are given in Appendix 2.

layers. The 16 nm layer deposited at 520 °C has some features in the AFM image, which the origin is not known.



**Figure 3.1:** AFM images of CeO<sub>2</sub> reference layers in different thicknesses deposited at 420 °C (top) and 520 °C (bottom). Image size is 2 x2 μm<sup>2</sup> and image depth is 4 nm.

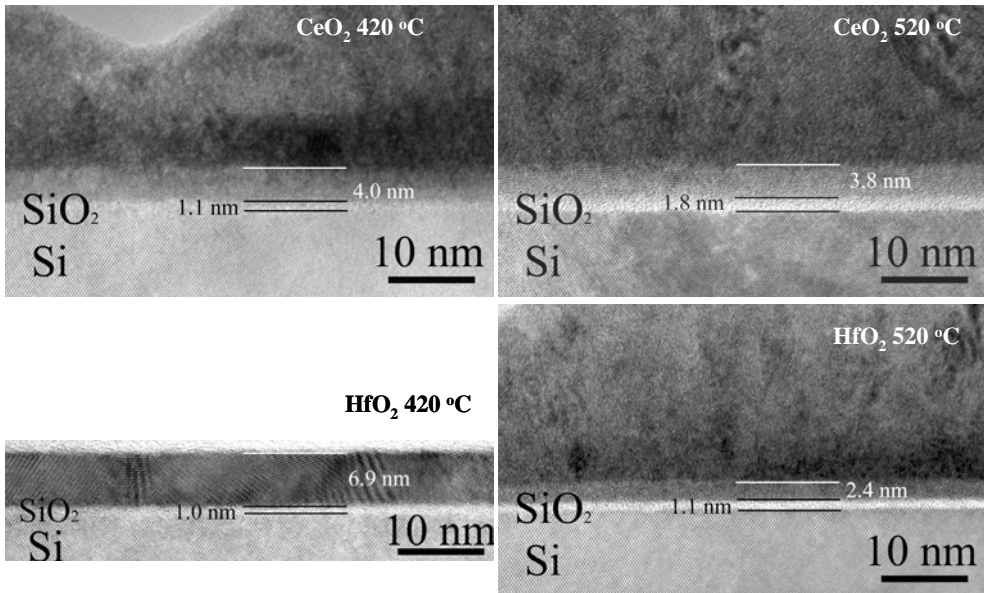
AFM images of the HfO<sub>2</sub> reference layers deposited at 420 and 520 °C are presented in Figure 3.2<sup>4</sup>. In contradiction to the results of CeO<sub>2</sub> layers, smoothness of the HfO<sub>2</sub> layers is found different for two different deposition temperatures. The layers deposited at 520 °C found to be smoother than those deposited at 420 °C. The origin of the features observed in the 12 nm layer deposited at 420 °C is not known.



**Figure 3.2:** AFM images of the HfO<sub>2</sub> reference layers in different thicknesses deposited at 420 °C (top) and 520 °C (bottom). Image size is 2 x2 μm<sup>2</sup> and image depth is 4 nm.

<sup>4</sup> AFM image of the 8 nm HfO<sub>2</sub> reference layer deposited 420 °C is not available.

Cross sectional TEM images of the  $\text{CeO}_2$  and  $\text{HfO}_2$  reference layers are presented in Figure 3.3<sup>5</sup>. Interface oxide thicknesses of the layers are found to be higher for the ones deposited at 520 °C compared to 420 °C and thinner for  $\text{HfO}_2$  than  $\text{CeO}_2$  layers. The TEM analysis showed that the layers deposited at 520 °C have thicker interfaces.

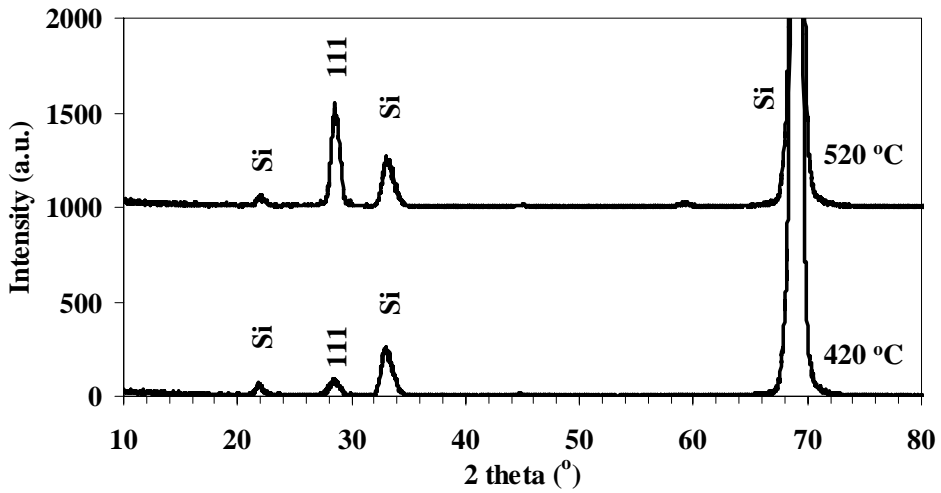


**Figure 3.3:** Cross sectional TEM images of the  $\text{CeO}_2$  (top), and  $\text{HfO}_2$  (bottom) reference layers deposited at 420 °C (left), and 520 °C (right). The top layer is TaN electrode, which is not present in  $\text{HfO}_2$  deposited at 420 °C.

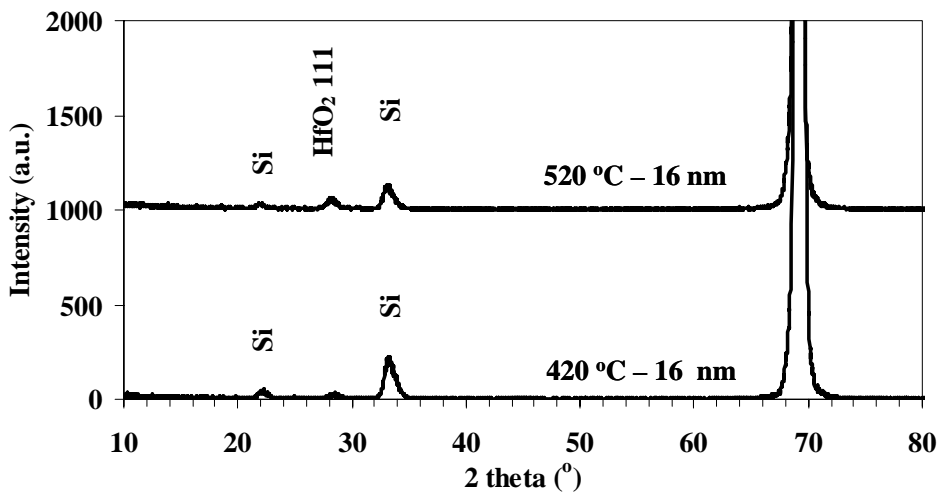
TEM analysis also showed that the  $\text{HfO}_2$  layer deposited at 520 °C is amorphous whereas the  $\text{HfO}_2$  layer deposited at lower temperature (420 °C) is already crystalline. This can be explained with the lower thickness of the layer, *i.e.* low surface to interface ratio, which increases the stability of amorphous phase [23-24]. The interface oxide of the  $\text{HfO}_2$  layers is thinner than the  $\text{CeO}_2$  layers. This difference is more obvious at 520 °C deposition temperature. Note that, the TEM image of  $\text{HfO}_2$  layer deposited at 420 °C is not from the area where the TaN electrode is present. This may lead a wrong conclusion about the interface oxide thickness of this layer, since the interface oxide is found to be thicker for the areas without a capping layer during electrode processing<sup>6</sup>. The TaN electrode layer, with a thickness of 100 nm, is polycrystalline according to the TEM images.

<sup>5</sup> Note that all images are with TaN electrode except  $\text{HfO}_2$  deposited at 420 °C, which has 8 nm deposited thickness, where the others are 4 nm.

<sup>6</sup> See Chapter 5 for details of the interface oxide thickness change during electrode processing.



**Figure 3.4:** XRD patterns of 16 nm CeO<sub>2</sub> reference layers deposited at 420 °C (bottom) and 520 °C (top).

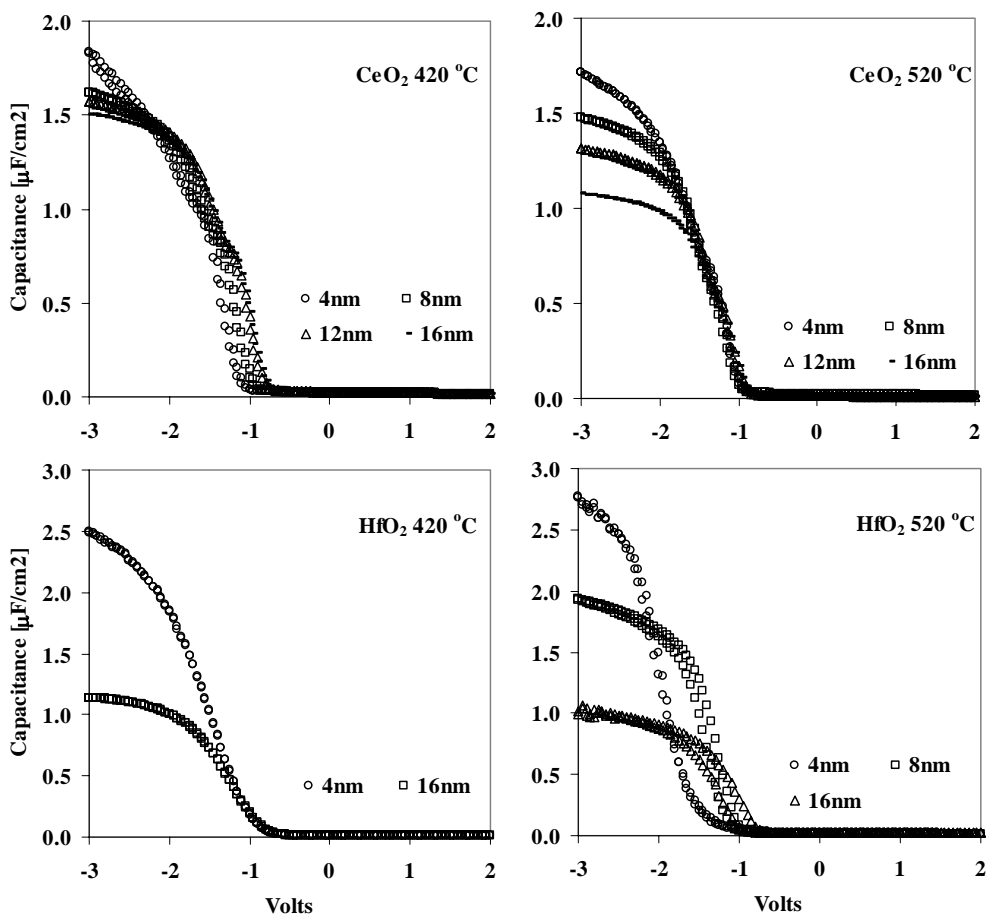


**Figure 3.5:** XRD patterns of 16 nm HfO<sub>2</sub> reference layers deposited at 420 °C (bottom) and 520 °C (top).

XRD analysis of CeO<sub>2</sub> and HfO<sub>2</sub> reference layers with 16 nm thickness deposited at 420 and 520 °C are presented in Figure 3.4 and 3.5, respectively. Analysis showed that both oxides have (111) orientation for both deposition temperatures, but the crystallinity of the layers is higher for 520 °C deposition temperature, as expected.

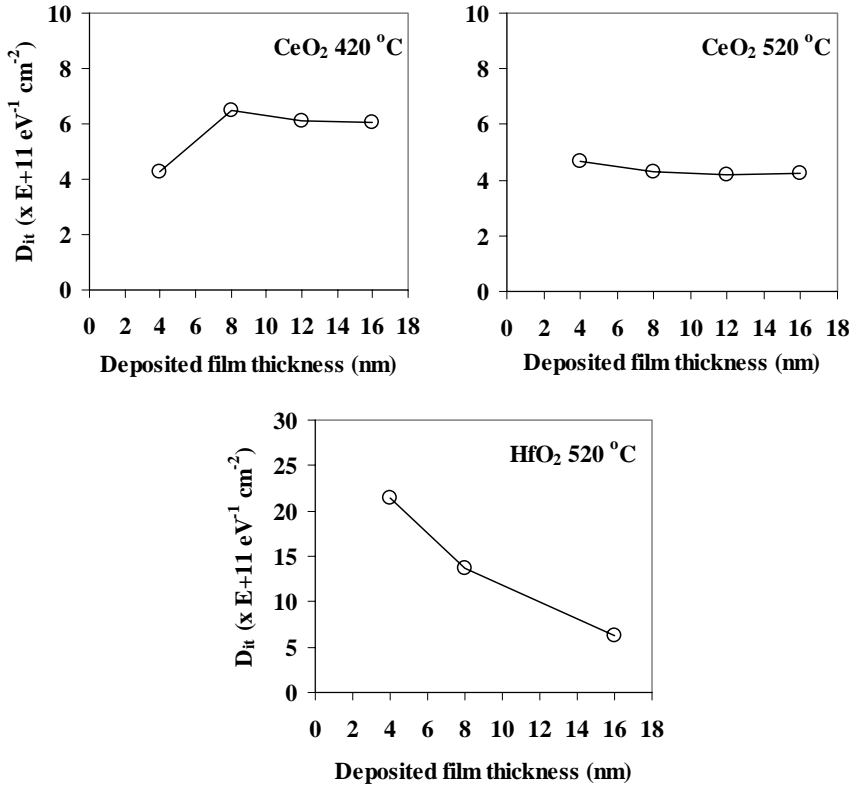
## Electrical Characterization

C-V plots of  $\text{CeO}_2$  and  $\text{HfO}_2$  reference layers deposited at 420 and 520 °C are presented in Figure 3.6. The figure shows that C-V curves of the  $\text{CeO}_2$  layers deposited at 420 °C have a shift to positive voltages with increasing thickness, similar to  $\text{HfO}_2$  reference layers deposited at 520 °C. It's also noted that  $\text{HfO}_2$  layers deposited at 520 °C shows a hysteresis, increasing by the layer thickness (in level 200 mV for the 16 nm layer). The hysteresis of the  $\text{CeO}_2$  layers for both deposition temperatures, as well as the  $\text{HfO}_2$  layers deposited at 420 °C, is found to be quite low (<50 mV).



**Figure 3.6:** C-V plots of the  $\text{CeO}_2$  (top) and  $\text{HfO}_2$  (bottom) reference layers deposited at 420 °C (left) and 520 °C (right).





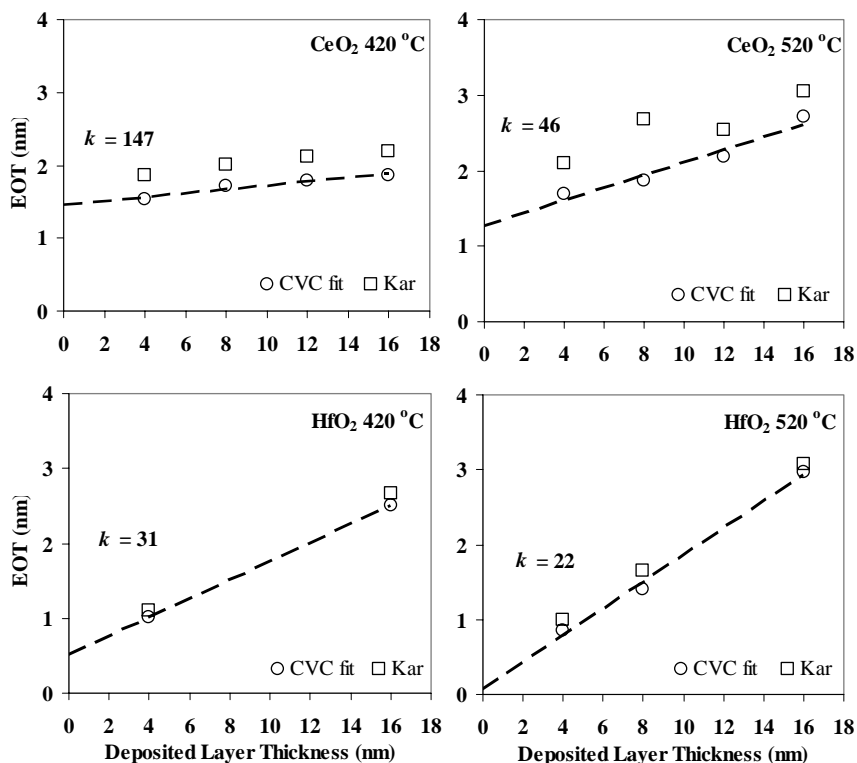
**Figure 3.7:**  $D_{it}$  values of  $\text{CeO}_2$  (top) and  $\text{HfO}_2$  (bottom) reference layers deposited at 420 and 520  $^\circ\text{C}$ , as a function of the layer thicknesses.

$\text{EOT}^7$  versus deposited layer thickness plots in Figure 3.8 are used for extracting the dielectric constant of the reference layers, and interface oxide thicknesses as well. Dielectric constant of the  $\text{CeO}_2$  layers deposited at 420  $^\circ\text{C}$  is found to be  $k=147$ , which is extremely high compared to the literature data of  $k=26$ .  $\text{CeO}_2$  reference layers deposited at 520  $^\circ\text{C}$  have a  $k=46$ , which is also higher than the theoretical value.

It can be seen that  $\text{HfO}_2$  layers in general, have thinner interface oxide<sup>8</sup> and it's found to be almost zero ( $\text{EOT}_{\text{IL}}=0.07 \text{ nm}$ ) for the layers deposited at 520  $^\circ\text{C}$ . This shows the efficiency of reducing ambient deposition on reducing the interface oxide thickness. The lack of data points of the  $\text{HfO}_2$  layers deposited at 420  $^\circ\text{C}$  makes difficult to draw a solid conclusion about the dielectric constant of the layers and the interface oxide thickness. Permittivity of the  $\text{HfO}_2$  layers deposited at 520  $^\circ\text{C}$  ( $k=22$ ) is in good agreement with literature data.

<sup>7</sup> EOT of the layers are extracted from their C-V analyses by using CVC simulation and the Kar method, which are described in details in Appendix 1.

<sup>8</sup> Interface oxide thickness extracted by this method shows the EOT of the interface oxide ( $\text{EOT}_{\text{IL}}$ ) instead of its physical thickness.



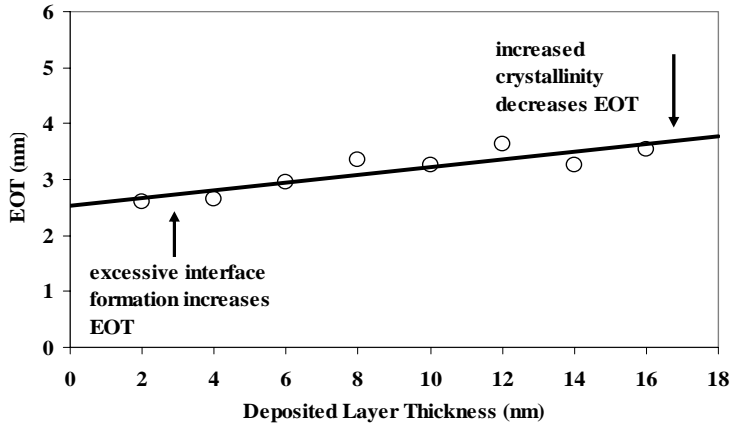
**Figure 3.8:** EOT versus deposited layer thickness of CeO<sub>2</sub> (top), and HfO<sub>2</sub> (bottom) reference layers deposited at 420 °C (left), and 520 °C (right). Dashed line shows the linear fit of the data, which is used for extracting  $k$  value from its slope.

The anomaly in the  $k$  values of CeO<sub>2</sub> layers, in particular the ones deposited at 420 °C, is related with a morphological change with increasing thickness, *i.e.* crystallization and/or preferred orientation, which is also observed for the laminated structures (see Chapter 4). EOT of the layers deposited at reducing ambient and oxidized by in-situ PDA, is affected by the layer thickness by two mechanisms:

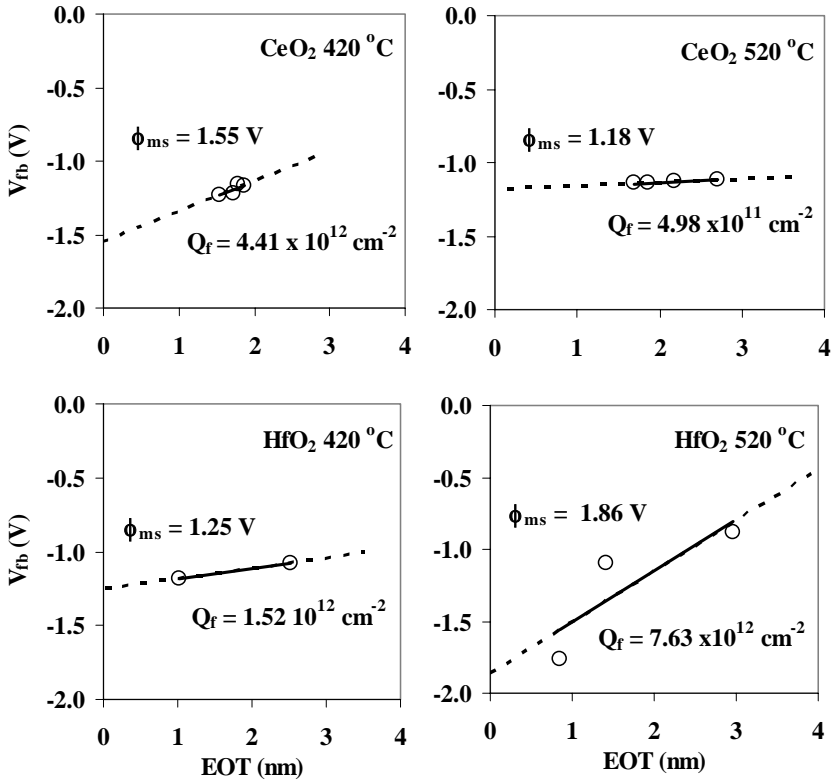
- Excessive oxidation of the interface for thinner layers due to high amount of oxygen diffusion towards interface. This increases the volume ratio of interface in the whole dielectric stack, hence, causes an increase in the EOT.
- Increased crystallinity by the increasing thickness. A transition from amorphous to crystalline phase causes an increase in dielectric constant and decreases the EOT. Additionally a preferred orientation may also cause an increase in the dielectric constant. Another possible effect of the crystallinity is on the conductance of the layers, mainly from to the grain boundaries in polycrystalline structure. Dual frequency series resistance correction<sup>9</sup> of the  $C$ - $V$  data is directly related with the conductance of the layers. In case of very high conductance (*i.e.* very high

<sup>9</sup> See Appendix 1 for detailed information about series resistance correction.

dissipation factor), the series resistance correction gives higher capacitance than actual, hence, may cause an error in EOT extraction.



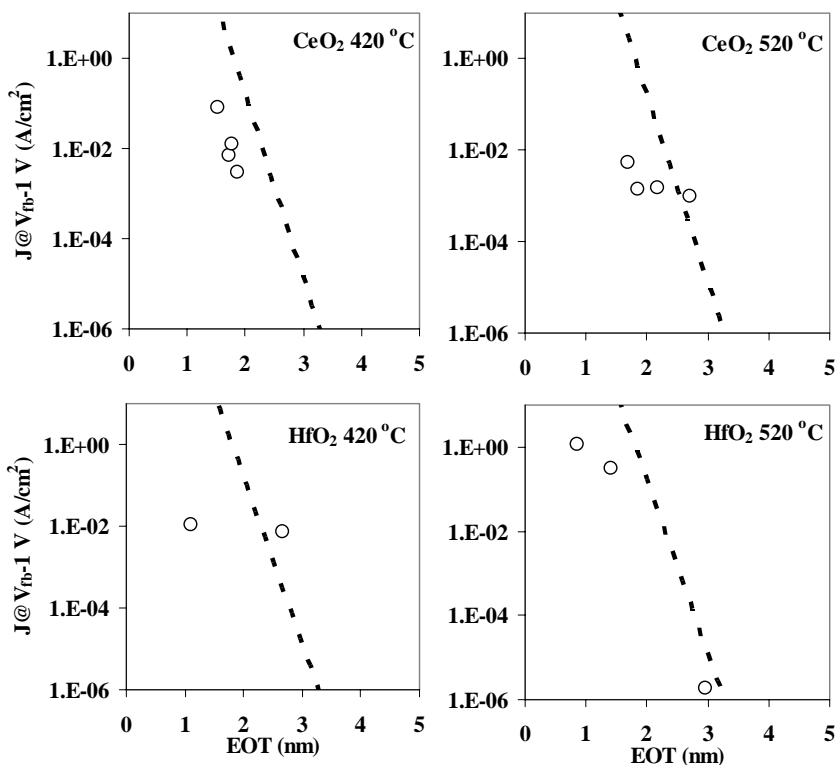
**Figure 3.9:** Effect of excessive interface oxidation and crystalline phase formation on the slope of the linear fit, which the dielectric constant is extracted from.



**Figure 3.10:**  $V_{fb}$ -EOT plots of CeO<sub>2</sub> (top), and HfO<sub>2</sub> (bottom) reference layers deposited at 420 °C (left), and 520 °C (right). Solid lines are the linear fit of the data and intersection of the linear fit gives the work function difference of the TaN electrode on given dielectric.

Effect of these two mechanisms on the slope of the linear fit of EOT vs. deposited layer thickness is illustrated in Figure 3.9. Note that a decrease in the slope of the linear fit results in wrong estimation of the electrical equivalent of the interface oxide thickness as well.

$V_{fb}$  versus EOT plots of the reference layers, shown in Figure 3.10, are used for extracting oxide fixed charge density ( $Q_f$ ) and work function difference ( $\phi_{ms}$ ). According to the plots and calculations based on them,  $CeO_2$  layers deposited at 520 °C have the lowest  $Q_f$  ( $Q_f=4.98 \times 10^{11} \text{ cm}^{-2}$ ), whereas the  $HfO_2$  layers deposited at the same temperature have the highest  $Q_f$  ( $Q_f=7.62 \times 10^{12} \text{ cm}^{-2}$ ). However, data belong to these layers have high scattering along the linear fit, which may cause errors in interpretations. Positive slope for all layers indicates the presence of negative charges in layers.



**Figure 3.11:** Leakage current densities measured at 1 V beyond  $V_{fb}$  ( $J$  at  $V_{fb}-1\text{V}$ ) and at -2 V of the  $CeO_2$  (top), and  $HfO_2$  (bottom) reference layers deposited at 420 °C (left), and 520 °C (right). Dashed lines are  $SiO_2$  reference data.

Leakage current density ( $J$ ) characteristics of the  $CeO_2$  and  $HfO_2$  reference layers are presented in Figure 3.11. According to the figure,  $CeO_2$  layers deposited at

420 °C and HfO<sub>2</sub> layers deposited at 520 °C have better leakage current reduction characteristics through increased EOT.

### **3.4. Conclusions**

The structural and electrical properties of the CeO<sub>2</sub> and HfO<sub>2</sub> layers deposited at 420 and 520 °C in reducing ambient are investigated.

- TEM and XRD analyses of the reference layers showed that the crystallinity of the single CeO<sub>2</sub> and HfO<sub>2</sub> layers are thickness dependent. For low thicknesses, the amount of the amorphous phase is more than crystalline in the layers. As the thickness increases, the layers evolve to a fully polycrystalline structure with a preferred orientation according to the XRD data.
- Interface oxide thickness of the CeO<sub>2</sub> layers is more than the HfO<sub>2</sub> layers for both deposition temperatures. Interface oxide thickness is found lower for 420 °C deposited layer than those deposited at 520 °C.
- HfO<sub>2</sub> layers deposited at 520 °C have more trapped charge in the layers compared to the other layers, as understood from *C-V* hysteresis.
- Dielectric constants of the layers extracted from the EOT-thickness plots showed an unrealistic *k* value (*k*=147) for the CeO<sub>2</sub> layers deposited at 420 °C, which is explained by the thickness dependent changes in the layer morphology. The dielectric constants of CeO<sub>2</sub> deposited at 520, HfO<sub>2</sub> deposited at 420 and 520 °C are found to be 46, 31 and 22, respectively.
- HfO<sub>2</sub> layers have the highest amount of interface states and their *D<sub>it</sub>* decreases with increasing HfO<sub>2</sub> thickness. *D<sub>it</sub>* of the CeO<sub>2</sub> reference layers showed a decrease for the increased deposition temperature, and found to be independent from the layer thickness, particularly for the CeO<sub>2</sub> layers deposited at 520 °C.
- *Q<sub>f</sub>* of the reference layers showed that the CeO<sub>2</sub> layers deposited at 520 °C have the lowest *Q<sub>f</sub>*= 4.98 x 10<sup>11</sup> cm<sup>-2</sup>, whereas the HfO<sub>2</sub> layers deposited at the same temperature have the highest *Q<sub>f</sub>*= 7.63 10<sup>13</sup> cm<sup>-2</sup>.
- The best EOT-*J<sub>g</sub>* trade-off is achieved in HfO<sub>2</sub> layers deposited at 520 °C. The CeO<sub>2</sub> reference layers deposited at 520 °C didn't show a leakage current reduction through EOT, which also can be correlated to the thickness dependency of the crystallinity of the layers.

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# *Chapter 4*

## **CeO<sub>2</sub> / HfO<sub>2</sub> Nanolaminates**

### **Abstract**

This chapter discusses the properties of CeO<sub>2</sub>/HfO<sub>2</sub> laminated dielectrics deposited by Pulsed Laser Deposition (PLD). The basic lamination parameters as the layer sequence and the individual layer thickness in the laminated structure are presented. The effects of the processing parameters like deposition ambient, deposition temperature, cooling rate during post deposition anneal (PDA), oxidation time in PDA on electrical and structural properties are investigated in detail.

It is found that the laminates with different layer sequences result in significant differences in electrical and morphological properties. Laminates starting with CeO<sub>2</sub> layer have better leakage current characteristics than those starting with HfO<sub>2</sub>, as well as lower EOT and lower interface state density. This is correlated to the different silicon-oxide interface properties and different crystallinity of the laminates with two different layer sequences.

## 4.1. Introduction

Mixing of oxides is a suitable technique to improve their electrical properties and structural properties on silicon [1-6]. Mixtures of HfO<sub>2</sub> with Dy<sub>2</sub>O<sub>3</sub> [7], Y<sub>2</sub>O<sub>3</sub> [8], TiO<sub>2</sub> [9, 10] and CaO [11] are some examples of HfO<sub>2</sub> based ternary oxides in literature. Though, a majority of the HfO<sub>2</sub> based ternary oxides research is concentrated on aluminates (HfAlO<sub>x</sub>) [12-20] and silicates (HfSiO<sub>x</sub>) [21-25]. Mixed oxide thin films of CeO<sub>2</sub>, which are not as pronounced as the mixed oxides of HfO<sub>2</sub>, as silicates (CeSiO<sub>x</sub>) [26], aluminates (CeAlO<sub>x</sub>) [27], lanthanates (CeLaO<sub>x</sub>) [28], zirconates (CeZrO<sub>x</sub>) [28-30] and hafnates (CeHfO<sub>x</sub>) [30] are reported in literature as well.

Another approach for multicomponent dielectric layers is depositing them in laminated structures by using the precise layering capabilities of the deposition methods as atomic layer deposition (ALD) [1, 31] and PLD [32]. Laminated structures, also known as nanolaminates, are proposed for improving the electrical properties (permittivity, leakage current and breakdown) of oxides [33- 48].

Effect of basic parameters of lamination, as the layer sequence and individual layer thickness and deposition ambient on the electrical and morphological properties of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates are discussed in the first section of this chapter. The effect of the deposition temperature is investigated by depositing a thickness series of laminates at various temperatures. Besides the direct effects of deposition temperature, *i.e.* the crystallinity of the layers, another important aspect is its effect on the oxidation kinetics of the laminates. In addition, the other parameters related to the *in-situ* PDA, like cooling rate and oxidation time, are also investigated. The properties of the laminates are compared with the binary oxides.

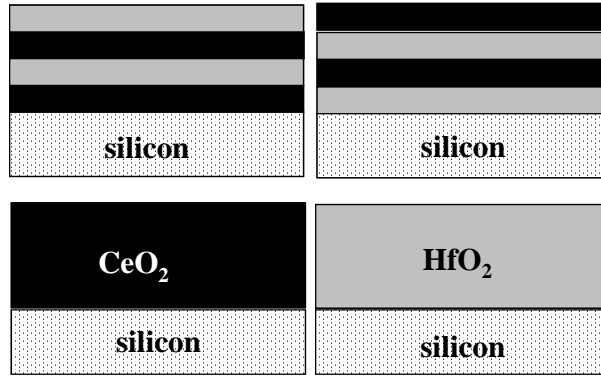
## 4.2. Layer Sequence in the Nanolaminates

In this section the effects of the layer sequence in the laminated structure are investigated. The properties of the two different layer sequences, CeO<sub>2</sub>-HfO<sub>2</sub>-CeO<sub>2</sub>-HfO<sub>2</sub> (C-H-C-H) and HfO<sub>2</sub>-CeO<sub>2</sub>-HfO<sub>2</sub>-CeO<sub>2</sub> (H-C-H-C), are compared with binary CeO<sub>2</sub> and HfO<sub>2</sub> layers with the same thickness<sup>1</sup>. Schematic representation of the layers is given in Figure 4.1.

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<sup>1</sup> From now on the layer sequence of CeO<sub>2</sub>-HfO<sub>2</sub>-CeO<sub>2</sub>-HfO<sub>2</sub> will be called as C-H-C-H laminate, whereas the other layer sequence of HfO<sub>2</sub>-CeO<sub>2</sub>-HfO<sub>2</sub>-CeO<sub>2</sub> as H-C-H-C laminate.





**Figure 4.1:** Schematic representation of laminated layers with two different sequences of CeO<sub>2</sub> and HfO<sub>2</sub> layers (top left and right) and binary HfO<sub>2</sub> and CeO<sub>2</sub> layers in the same thickness (bottom left and right).

#### 4.2.1. Experimental

Both, binary CeO<sub>2</sub> and HfO<sub>2</sub> layers and CeO<sub>2</sub>-HfO<sub>2</sub> laminates with two different layer sequences, are deposited by PLD on hydrogen passivated silicon. Substrates are annealed at deposition temperature for 15 minutes at 0.1 mbar Ar+H<sub>2</sub> pressure with a gas flow rate of 30 ml/min, prior to deposition<sup>2</sup>.

The thickness of the laminated and binary layers was 4 nm. The laminated structure consists of two different types of layer sequence, *i.e.* C-H-C-H and H-C-H-C, with an individual layer thickness of 1 nm. Layers are deposited at 420 °C, in 0.1 mbar Ar+H<sub>2</sub> and from CeO<sub>2</sub> and HfO<sub>2</sub> targets by using an energy density of 1 and 3 J/cm<sup>2</sup>, respectively. Deposition is followed by an *in-situ* high pressure oxygen post deposition anneal (PDA)<sup>3</sup>. The only difference between pure oxides and two different laminates were the cooling rates during PDA: Cooling rate for laminates was 2 °C/min, for pure oxides was 5 °C/min.

Au by sputtering via a shadow mask *and* TaN by sputtering followed by lithography and dry etching, are performed for preparing MOS devices<sup>4</sup>.

The structural properties of the layers are characterized by atomic force microscope (AFM), X-Ray photoelectron spectroscopy (XPS), X-Ray diffraction (XRD) and transmission electron microscope (TEM) analyses. Capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements are performed for electrical characterization of the layers.

<sup>2</sup> See Chapter 2, Section 2.3.1 for details of substrate annealing.

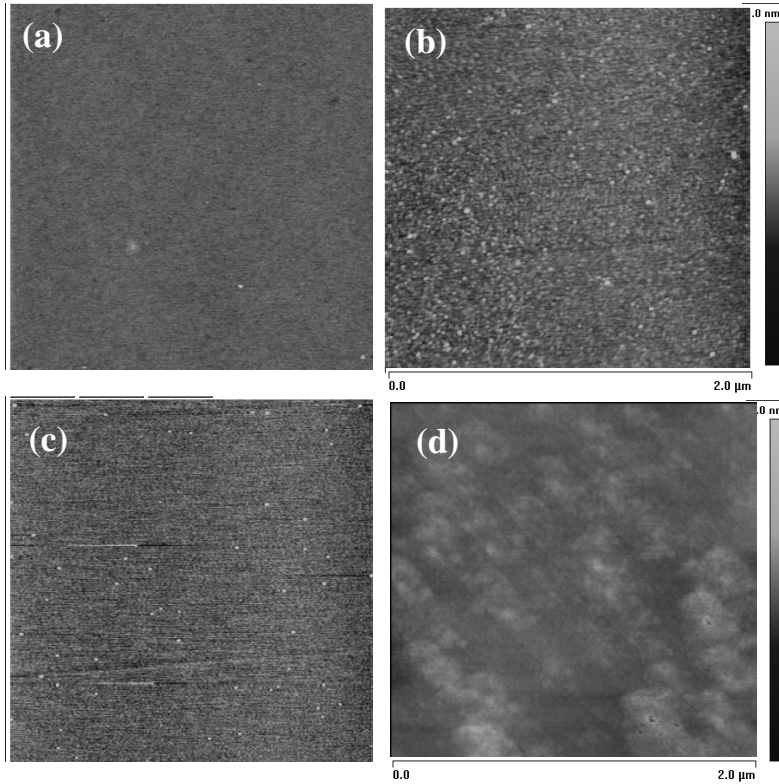
<sup>3</sup> See Chapter 2 for details of reducing ambient deposition followed by *in-situ* PDA

<sup>4</sup> See Appendix 2 for details of electrode depositions and MOS device processing

## 4.2.2. Results and Discussion

### *Structural Characterization*

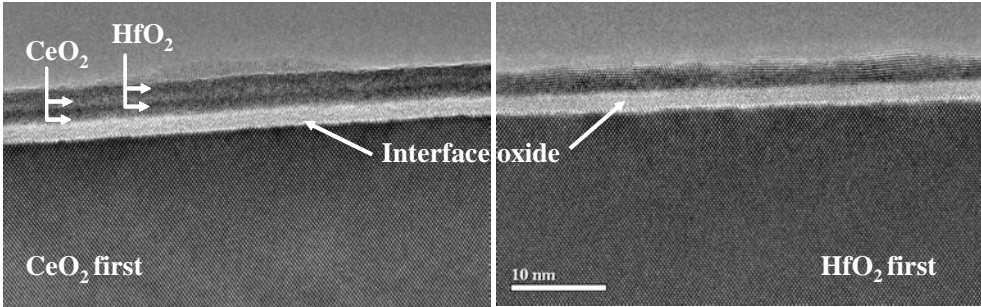
AFM images of the layers with 4 nm deposited thickness, deposited at 420 °C in 0.1 mbar Ar+H<sub>2</sub> ambient are presented in Figure 4.2. The major difference between the layers is the features observed in the laminated structure starts with HfO<sub>2</sub> layer (Figure 4.2.d). It is also noted that the CeO<sub>2</sub> layer presented in Figure 4.6.a has a surface smoothness close to the substrate.



**Figure 4.2:** AFM images of the 4 nm layers deposited at 420 °C in 0.1 mbar Ar+H<sub>2</sub> ambient. (a) CeO<sub>2</sub> (b) HfO<sub>2</sub> (c) C-H-C-H laminate (d) H-C-H-C laminate. (Image size is 2x2 μm and depth scale is 4 nm)

Cross sectional TEM images (Figure 4.8) of the two different layer sequences shows the presence of crystallites in the H-C-H-C laminate, whereas the C-H-C-H laminate layer remains amorphous and the individual CeO<sub>2</sub> and HfO<sub>2</sub> layers can be clearly distinguished. The presence of crystallites in the H-C-H-C laminate explains the features observed in its AFM image too. Fast Fourier Transformation (FFT) analysis on more detailed TEM images (Figure 4.4) showed that the crystallites formed in the H-C-H-C laminate are in tetragonal CeHfO<sub>4</sub> structure. Results of this analysis are shown in

Table 4.1. The TEM images also showed that the interface layer thickness is slightly thinner (1.4 nm) in the H-C-H-C laminate than the C-H-C-H laminate (1.7 nm).

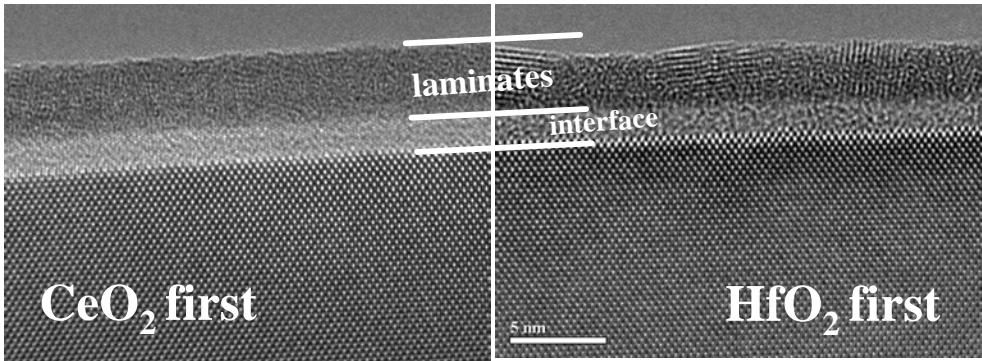


**Figure 4.3:** Cross sectional TEM images of the laminates with two different layer sequences. Separate layers are visible in C-H-C-H sequence in amorphous structure (left), as the H-C-H-C sequence has crystallites (scale bar is 10 nm).

The FFT derived crystal data of the crystallites in H-C-H-C laminate fits to (101) textured CeHfO<sub>4</sub> structure. However, it's noted that this structure is nearly identical to (111) cubic CeO<sub>2</sub> structure in manner of interplanar distances. The tetragonal structure is achieved by a slight deformation of the cubic lattice, which is highly probable due to presence of Hf in the structure. Formation of the tetragonal phase in CeO<sub>2</sub>-HfO<sub>2</sub> solid solutions by internal distortion of fluorite phase is also reported in literature [49].

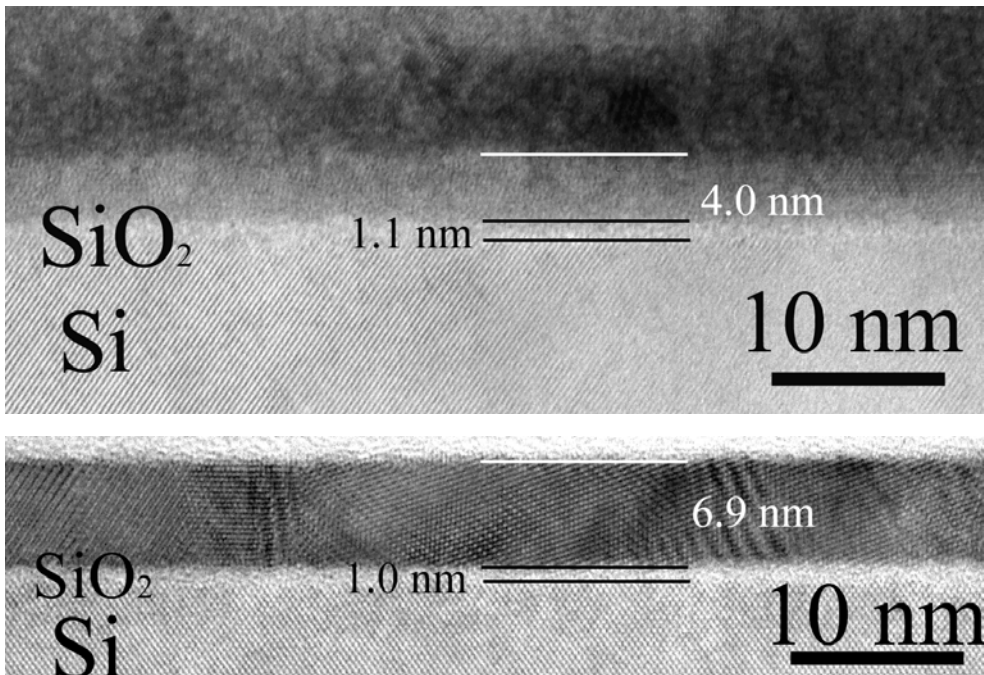
**Table 4.1:** Comparison of the FFT derived interplanar distances of the crystallites observed in the H-C-H-C laminate with the crystal data.

H-C-H-C Laminate			Literature data		
			CeO <sub>2</sub> 81-0792	HfO <sub>2</sub> 83-0808	CeHfO <sub>4</sub> 47-0493
[0-11]	[010]	[010]	← viewed along zone-axis		
			3.1248	---	---
3.08	3.04±0.02	3.06±0.01	---	---	3.0642
			---	2.9423	---
	2.66	2.59	2.7062	2.6138	2.6603
1.86	1.88	1.90	1.9135	1.9065	1.8822
			1.5624	1.5650	---
CeHfO <sub>4</sub>	CeHfO <sub>4</sub>	CeHfO <sub>4</sub>			



**Figure 4.4:** Detailed TEM images of laminates with two different layer sequence. C-H-C-H sequence (left) is amorphous as the H-C-H-C sequence (right) has crystallites.

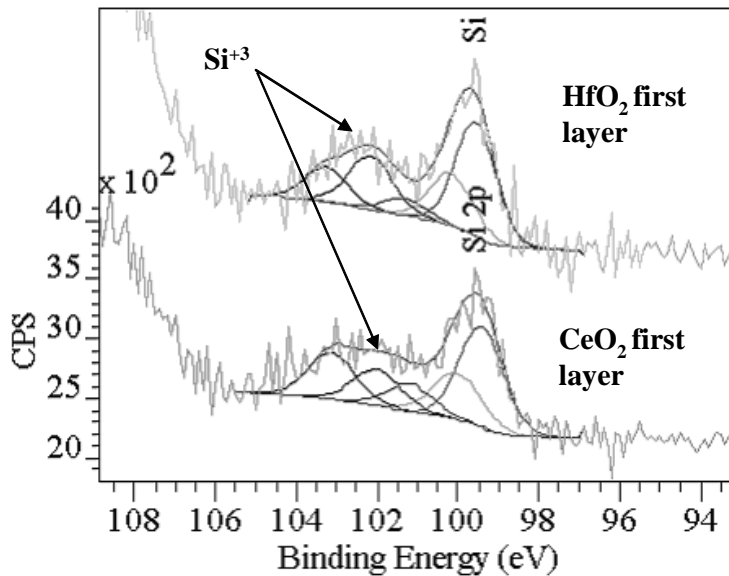
TEM images of the  $\text{CeO}_2$  and  $\text{HfO}_2$  layers are presented in Figure 4.5. It's noted that, both,  $\text{CeO}_2$  and  $\text{HfO}_2$  are not amorphous: The  $\text{CeO}_2$  layer has small crystallites, whereas the  $\text{HfO}_2$  layer is completely polycrystalline. Note that, the thickness of  $\text{HfO}_2$  layer presented here is not 4 nm but the 8 nm layer (deposited thickness estimation) instead, which may affect the crystallinity of the layer. The figure also shows a very thin interface ( $< 1$  nm) for  $\text{HfO}_2$  layer.



**Figure 4.5:** TEM images of  $\text{CeO}_2$  (top) and  $\text{HfO}_2$  (bottom) layers grown at 420 °C, in 0.1 mbar  $\text{Ar}+\text{H}_2$  ambient.

A comparison of the two different CeO<sub>2</sub>-HfO<sub>2</sub> layer sequence laminates with the CeO<sub>2</sub> and HfO<sub>2</sub> layers shows that the C-H-C-H laminate is the only totally amorphous one. This leads to the conclusion that the Si-HfO<sub>2</sub> interface is more favorable to form crystalline phase than the Si-CeO<sub>2</sub> interface. The stability of the amorphous phase is higher in laminated structures. Although the pure CeO<sub>2</sub> layer has the same interface characteristics as the C-H-C-H laminate, the increased stability of the amorphous phase in laminated structure can be explained by diminishing the nucleation of a crystalline CeO<sub>2</sub> phase by insertion of an HfO<sub>2</sub> layer. Since the amorphous stability of HfO<sub>2</sub> increases with low surface to interface area [50, 51], as in the case of HfO<sub>2</sub> layer of 1 nm in thickness in laminated structures, HfO<sub>2</sub> layer deposited on top of amorphous CeO<sub>2</sub> layer supposed to remain amorphous as well.

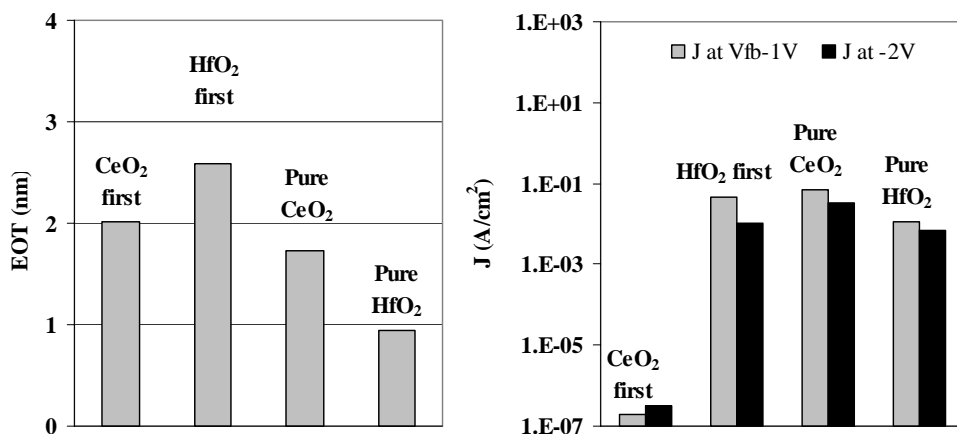
XPS analyses of Si 2p peaks of the laminates are presented in Figure 4.6. The Si<sup>+3</sup> states are more pronounced in the H-C-H-C sequence laminates compared to the other layer sequence. This means that the Si-HfO<sub>2</sub> interface contains more interface states than the Si-CeO<sub>2</sub> interface, which is also observed in  $D_{it}$  measurements (see *Electrical Characterization* part in this section).



**Figure 4.6:** XPS analyses of Si 2p peaks of two different layer sequence laminates; H-C-H-C (top) and C-H-C-H (bottom). Inner curves show the simulations based on the measurement data at the outermost of the spectra.

Electrical Characterization<sup>5</sup>

Equivalent oxide thicknesses (EOT) and leakage current densities ( $J$ ) at 1 V beyond flatband voltage ( $V_{fb}$ ) and at -2 V, of the laminates, compared with  $\text{CeO}_2$  and  $\text{HfO}_2$  layers of the same thickness (4 nm) are presented in Figure 4.7. EOT and  $V_{fb}$  of the dielectrics are extracted by CVC simulation. According to the figure,  $\text{HfO}_2$  has the lowest EOT=0.95 nm, whereas the H-C-H-C laminate with has the highest EOT=2.58 nm. Leakage current density characteristics of the compared layers are showing that the C-H-C-H laminate has a significant low leakage current compared the other laminate and the  $\text{CeO}_2$  and  $\text{HfO}_2$  reference layers. Although the cooling rates during PDA for laminates and pure oxides were different (2 °C/min for laminates, 5 °C/min for binary oxides), significant leakage current reduction is clearly visible for the laminate that has C-H-C-H compared to the other lamination sequence. Difference of cooling rates may lead two different interface oxide thicknesses, which has a direct effect on leakage current properties. However, TEM analysis of laminated structures, comparing 2 and 10 °C/min cooling rates<sup>6</sup>, showed that the interface oxide thickness is not changing significantly. In general, for the laminates deposited at 520 °C, a lower cooling rate during PDA results in lower interface state density ( $D_{it}$ ) compared to the high cooling rates, which results in better leakage current characteristics.



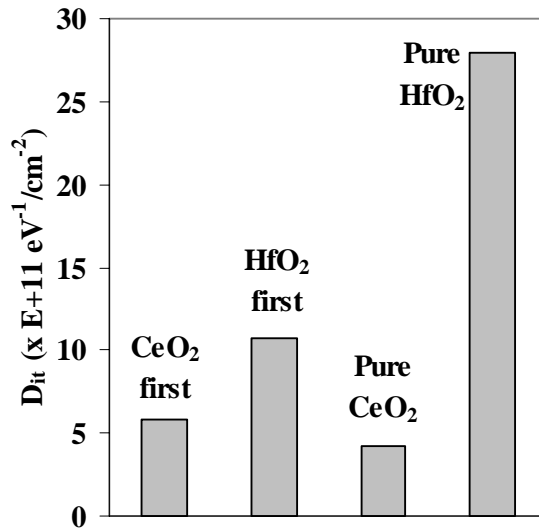
**Figure 4.7:** EOT (left) and leakage current densities (right) of laminated oxides with two different layer sequences, compared with pure  $\text{CeO}_2$  and  $\text{HfO}_2$  with the same thickness, deposited at 420 °C at 0.1 mbar  $\text{Ar}+\text{H}_2$ .

The  $D_{it}$  values of the layers compared here are presented in Figure 4.8. According to the figure  $\text{CeO}_2$  with a cooling rate of 5 °C/min during PDA, have the lowest  $D_{it}$  ( $4.26 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ ), whereas C-H-C-H laminate, which has the Si- $\text{CeO}_2$

<sup>5</sup> See Appendix 1 for details of the methods used for electrical characterization.

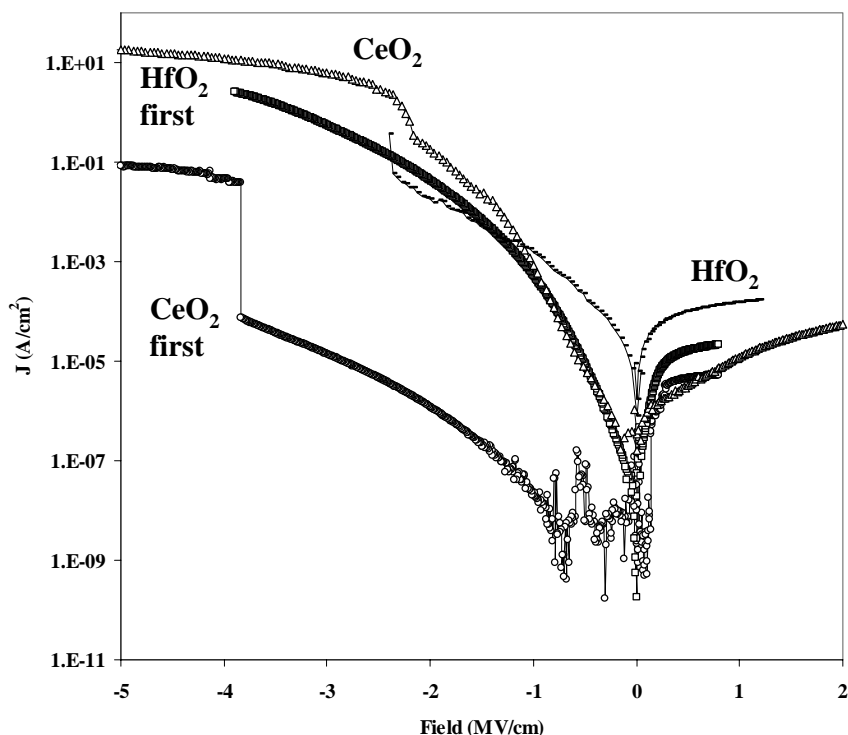
<sup>6</sup> Effects of cooling rate on laminated dielectrics are discussed in the Section 4.5 in this chapter.

interface as well, have a higher  $D_{it}$  ( $5.85 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ ). This seems like a contradiction comparing the dependency of  $D_{it}$  on cooling rate of laminated structures deposited at 520 °C. However, for a better evaluation of  $D_{it}$ , the difference in deposition temperatures has to be considered as well: Higher deposition temperature means higher oxygen diffusion rate during PDA, hence, higher sensitivity to the changes in cooling rate. Other possible structural changes (*i.e.* crystallinity) are also should be taken into account for different deposition temperatures. Therefore, it's not a contradiction to observe comparable  $D_{it}$  values for the layers grown at lower temperatures, since the effect of deposition temperature on  $D_{it}$  is lower for low deposition temperatures. In general, Si-HfO<sub>2</sub> interface seems like to form more interface states than Si-CeO<sub>2</sub> interface. This result is in good agreement with the XPS analysis, which showed more Si<sup>+3</sup> states H-C-H-C laminate than the other layer sequence.



**Figure 4.8:**  $D_{it}$  of laminated oxides with two different layer sequences, compared with the pure CeO<sub>2</sub> and HfO<sub>2</sub> with the same thickness deposited at 420 °C at 0.1 mbar Ar+H<sub>2</sub>.

$J$ - $E$  (leakage current density–electric field) characteristics of the layers are presented in Figure 4.9. The C-H-C-H laminate has the highest breakdown field of 3.8 MV/cm, as well as the lowest leakage current ( $J$  at  $V_{fb}-1 \text{ V} = 1.88 \times 10^{-7} \text{ A/cm}^2$ ). According to the electrical characteristics, laminated structures didn't give the best EOT but a considerable leakage current reduction is achieved in the laminated structure with C-H-C-H sequence.



**Figure 4.9:**  $J$ - $E$  plot of  $\text{CeO}_2$ - $\text{HfO}_2$  laminated dielectrics with two different layer sequences, compared with the single  $\text{CeO}_2$  and  $\text{HfO}_2$  with the same thickness deposited at  $420^\circ\text{C}$  at 0.1 mbar  $\text{Ar}+\text{H}_2$ .

In conclusion, the major structural and electrical characteristics of the compared layers are summarized as follows:

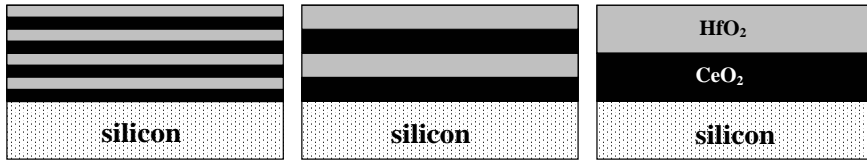
- The Si- $\text{HfO}_2$  interface is found to be improving crystallinity in the layers compared to the Si- $\text{CeO}_2$  interface.
- Laminated structure diminishes crystalline phase formation.
- Polycrystalline  $\text{HfO}_2$ , with the lowest interface thickness has the lowest EOT (0.95 nm).
- The only totally amorphous layer was the C-H-C-H laminate with an EOT of 2 nm, showed the lowest leakage current density ( $J$  at  $V_{fb}-1$  V =  $1.88 \times 10^{-7}$  A/cm<sup>2</sup>) and highest breakdown voltage (3.8 MV/cm).

### 4.3. Effect of the Lamination Degree and the Deposition Ambient

The degree of the lamination is defined as the number of layers in a laminated structure for a given thickness. As the individual layer thickness in the laminated structure decreases, the total number of the layers increases. For understanding the effect of lamination degree on the properties of the  $\text{CeO}_2$ - $\text{HfO}_2$  laminated dielectrics, total thickness of 8 nm is kept constant for all structures and individual layer thickness



is increased from 1 nm to 4 nm. By this way three different types of laminates are deposited: 8 x 1 nm, 4 x 2 nm and 2 x 4 nm, as shown schematically in Figure 4.10.



**Figure 4.10:** Schematic structure of three different laminated structure with different individual layer thicknesses. 8 x 1 nm (left), 4 x 2 nm (middle) and 2 x 4 nm (right).

Effect of the deposition ambient on the properties is also investigated by using Ar+H<sub>2</sub> and O<sub>2</sub> deposition ambient at the same pressure during the deposition of the layers.

#### 4.3.1. Experimental

8 nm layers in C-H-C-H sequence with different lamination degrees are deposited on hydrogen passivated silicon substrates and substrates are annealed at deposition temperature for 15 minutes at 0.1 mbar Ar+H<sub>2</sub> pressure with a gas flow rate of 30 ml/min, prior to deposition<sup>7</sup>. Layers are deposited at 520 °C, in 0.1 mbar Ar+H<sub>2</sub> and O<sub>2</sub> and deposition is followed by an *in-situ* high oxygen pressure PDA<sup>8</sup>. 1 and 3 J/cm<sup>2</sup> laser energy densities are used for CeO<sub>2</sub> and HfO<sub>2</sub> targets, respectively.

A second set of experiment was designed for understanding the effects of deposition ambient. CeO<sub>2</sub>-HfO<sub>2</sub> laminates, with an individual layer thickness of 1 nm are deposited to form a thickness series starting from 2 nm to 12 nm total thickness. The PLD parameters were the same as previous section.

Au electrodes via a shadow mask are deposited by sputtering to prepare MOS devices for electrical characterization.

#### 4.3.2. Results and Discussion

##### *Lamination Degree*

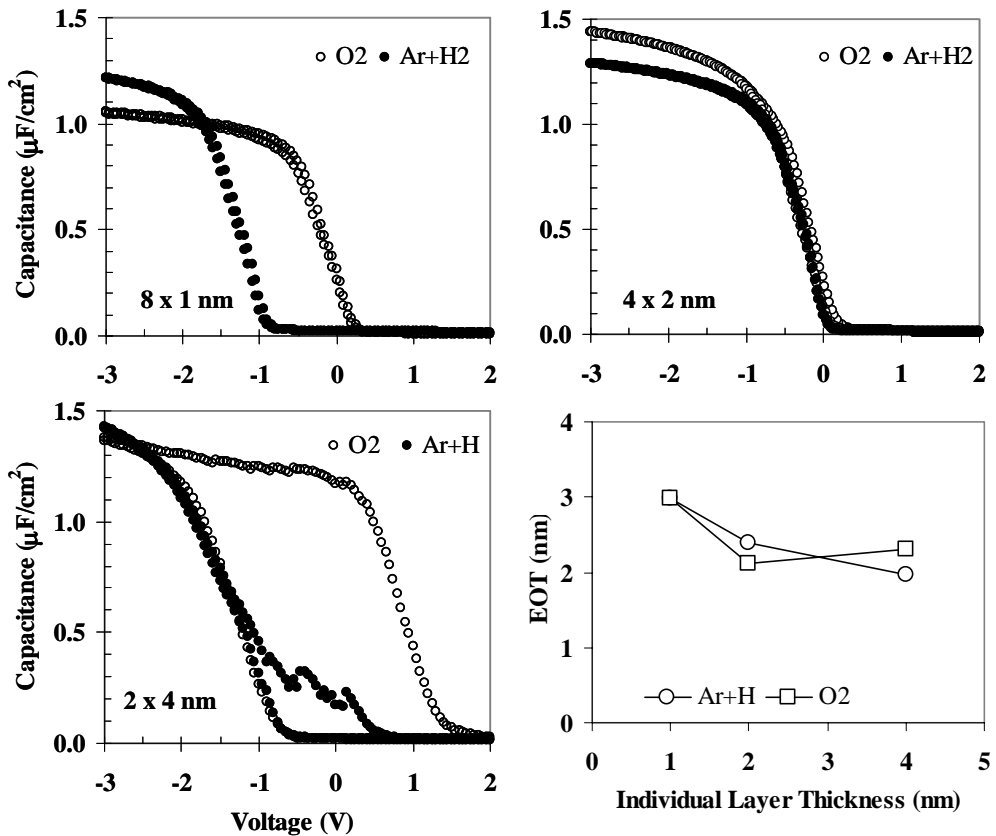
C-V plots and the extracted EOT values of the layers with different lamination degrees are presented in Figure 4.11. The C-V data shows a very large hysteresis in the laminate with 2 x 4 nm layers deposited in oxygen. Although the layers grown in oxygen have higher hysteresis comparing to those deposited in Ar+H<sub>2</sub>, a hysteresis of

<sup>7</sup> See also Chapter 2, section 2.3.1 for details of substrate pre-treatments.

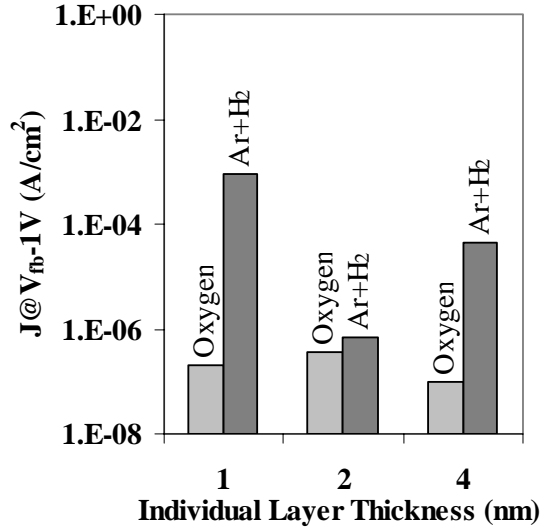
<sup>8</sup> See Chapter 2 for details of reducing ambient deposition followed by *in-situ* PDA.

2 V is significant. This indicates the presence of high amount of oxide trapped charges. The laminate with same lamination degree deposited in Ar+H<sub>2</sub> also shows a large hysteresis but this seems like a shoulder in *C-V* plot. As a general result, one can say that, as the individual layer thickness increases in laminate, the *C-V* hysteresis increases as well. This can be correlated by the possible presence of different phases in the laminates: Amorphous, CeHfO<sub>4</sub>, CeO<sub>2</sub> and HfO<sub>2</sub>. Formation of a crystalline phase is related with the individual layer thickness by changing the surface to volume ratio by means of increasing individual layer thickness.

Leakage current characteristics of the laminates with different lamination degrees are also compared and the results are presented in Figure 4.12. Laminates deposited in oxygen have lower leakage current densities compared to those deposited in Ar+H<sub>2</sub>. This can be explained by the increase in interfacial oxide layer thickness, as well as the difference in oxygen vacancies in the layers grown in oxygen.



**Figure 4.11:** *C-V* plots of three different lamination degree, with three different individual layer thicknesses of 1 nm (8 layers, top left), 2 nm (4 layers, top right) and 4 nm (2 layers, bottom left). Their EOT values extracted by CVC simulation are also shown (bottom right).



**Figure 4.12:**  $J$  at  $V_{fb}-1$  V of the laminates with different lamination degrees grown in O<sub>2</sub> and Ar+H<sub>2</sub>

In conclusion, 1 nm individual layers in the laminated structure is found to be advantageous than thicker ones for decreasing the  $C-V$  hysteresis. The layers deposited in O<sub>2</sub> have lower leakage current density than the ones deposited in Ar+H<sub>2</sub>, regardless from the lamination degree. However, the  $C-V$  hysteresis of the layers deposited in O<sub>2</sub>, which reaches up to  $\Delta V_{fb}=2$  V in 2 x 4nm layer, found much higher compared to the layers deposited in Ar+H<sub>2</sub>.

#### *Reducing vs. Oxidizing Deposition Ambient*

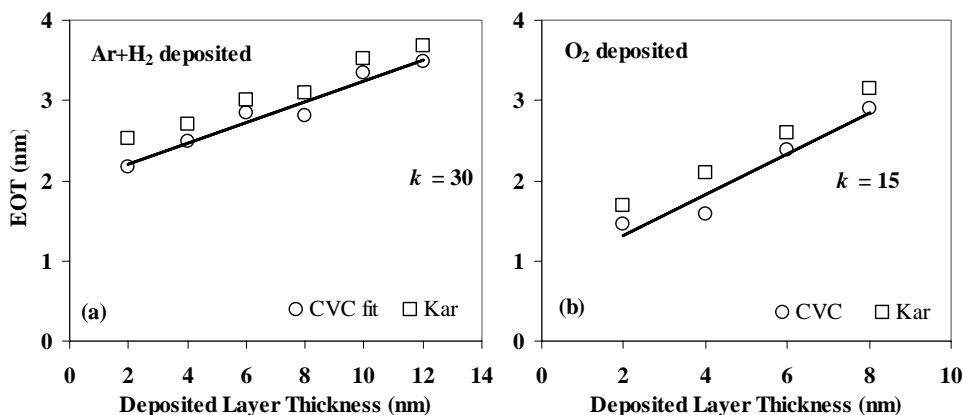
In order to understand the effect of deposition ambient in details, on the electrical properties of CeO<sub>2</sub>-HfO<sub>2</sub> laminates, another set of depositions was carried out. In this set of depositions, each layer thickness is kept at 1 nm and for a total laminate thickness of 2 nm to 12 nm. All layers are deposited at 520 °C with 0.1 mbar Ar+H<sub>2</sub> and O<sub>2</sub>, respectively.

The EOT values<sup>9</sup> of the layers are presented in Figure 4.13. There are two important aspects seen in this figure: First one is the low interface oxide thickness<sup>10</sup> of the layers grown in oxygen. Low interface oxide thickness of the laminates deposited in oxygen can be explained by two possible mechanisms: More stable interface oxide formation during deposition *or* intermixing of SiO<sub>2</sub> with the first layer of the laminate

<sup>9</sup> See Appendix 1 for details of the electrical characterization methods.

<sup>10</sup> Interface oxide thickness term is used to refer the electrical equivalent of physical thickness, extracted by  $C-V$  measurements

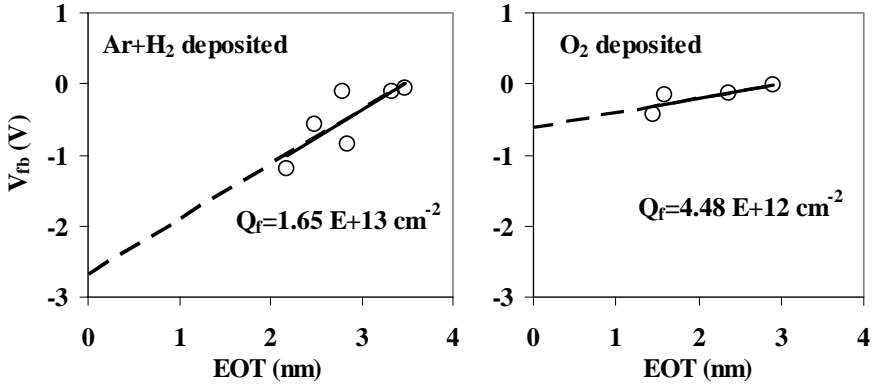
(CeO<sub>2</sub>). The second important aspect is the high permittivity ( $k=30$ ) of the layers grown in Ar+H<sub>2</sub>.



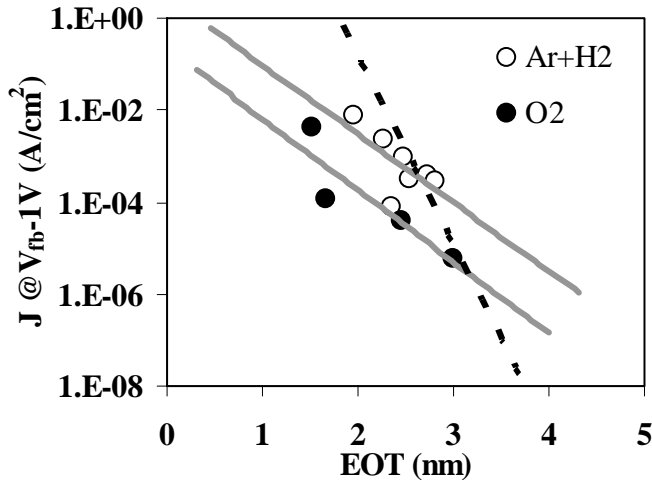
**Figure 4.13:** EOT versus deposited layer thickness of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates deposited in O<sub>2</sub> and Ar+H<sub>2</sub> at 520 °C. Lines show the linear fit of the data.

Major difference between two different deposition ambient is in the  $V_{fb}$  of the layers as shown in Figure 4.14. Layers deposited in O<sub>2</sub> have higher  $V_{fb}$  compared to those deposited in Ar+H<sub>2</sub>, which means the presence of more oxide fixed charges in layers deposited in Ar+H<sub>2</sub>. Slopes of the linear fit of  $V_{fb}$ -EOT plots indicate that the amount of fixed oxide charges is different;  $Q_f=1.65 \times 10^{13} \text{ cm}^{-2}$  for the layers deposited in Ar+H<sub>2</sub> and  $Q_f=4.48 \times 10^{12} \text{ cm}^{-2}$  for the layers deposited in O<sub>2</sub>. The difference in  $Q_f$  of the layers is correlated to the difference in oxygen vacancies in the layers. Another aspect from the  $V_{fb}$ -EOT plot of the layers is the two different work function differences ( $\phi_{ms}$ ), found from the intersection of the linear fit, for the layers deposited in Ar+H<sub>2</sub> ( $\phi_{ms}=-2.67 \text{ V}$ ) and in O<sub>2</sub> ( $\phi_{ms}=-0.62 \text{ V}$ ). This is correlated to the excessive amount of  $Q_f$  in the layers.  $V_{fb}$  is dominantly determined by  $Q_f$  and  $Q_{it}$  for values of  $Q_f + D_{it} > 10^{12} \text{ cm}^{-2}$ , hence, the high amount of oxide charges in the layers causes large differences in  $V_{fb}$  and therefore causes differences in the  $\phi_{ms}$  [52].

Leakage current characteristics of the laminates with different thicknesses are compared. Layers deposited in Ar+H<sub>2</sub> and O<sub>2</sub> have similar  $J$ - $E$  characteristics. However, as a general remark, breakdown voltages of the layers deposited in Ar+H<sub>2</sub> are found to be lower than those deposited in O<sub>2</sub>. The leakage current densities of the layers at accumulation voltages (at  $V_{fb}-1 \text{ V}$ ) show the main difference as indicated in Figure 4.15. The higher  $J$  of the layers deposited in Ar+H<sub>2</sub> is correlated to the higher amount of defects in the layers. Higher defect density causes higher leakage current density by trap assisted tunneling [53].



**Figure 4.14:**  $V_{fb}$ -EOT plots of the laminates deposited in Ar+H<sub>2</sub> (left) and O<sub>2</sub> (right). Lines are the linear fit of the data.



**Figure 4.15:** EOT- $J_g$  trade-off of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates deposited in Ar+H<sub>2</sub> and O<sub>2</sub>. Dashed line shows the SiO<sub>2</sub> reference data and solid lines in the figure are guide for eye purposes only.

In conclusion, the CeO<sub>2</sub>-HfO<sub>2</sub> laminates deposited in O<sub>2</sub> showed a better EOT- $J_g$  trade-off and lower  $Q_f$  than the layers deposited in Ar+H<sub>2</sub>. However, the dielectric constant of these layers was only  $k=15$ , whereas the laminates deposited in Ar+H<sub>2</sub> have a  $k=30$ . Since a  $k$  value of 15 was quite low for a high- $k$  material to meet the near future requirements, further research in this thesis is concentrated on CeO<sub>2</sub>-HfO<sub>2</sub> laminates deposited in Ar+H<sub>2</sub>. In particular, in the optimization of the oxidation of layers by *in-situ* PDA, and getting a closer control on their leakage current properties is aimed.

#### 4.4. Effect of Deposition Temperature

Effect of main parameters, as the structure of lamination (layer sequence and individual layer thickness) and deposition ambient on the electrical and morphological properties of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates were discussed previously in this chapter. In the first part of this section, the properties of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates with 4 nm thickness, deposited at various temperatures are compared. In the second part, a thickness series of the laminates deposited at 420, 520 and 620 °C are investigated and properties are compared with single CeO<sub>2</sub> and HfO<sub>2</sub> reference layers.

##### 4.4.1. Experimental

CeO<sub>2</sub>-HfO<sub>2</sub> laminates with various thicknesses, in C-H-C-H sequence with an individual layer thickness of 1 nm, are deposited on hydrogen passivated Si (001) substrates<sup>11</sup> at different temperatures (from 220 °C to 850 °C). The layers are deposited in 0.1 mbar Ar+H<sub>2</sub> (5%) gas mixture, with the PLD parameters given in Chapter 2. An *in-situ* PDA in high oxygen pressure (p<sub>O2</sub> = 100 mbar) with a cooling rate of a 5 °C/min is applied for all layers<sup>12</sup>.

##### 4.4.2. Results and Discussion

###### *CeO<sub>2</sub>-HfO<sub>2</sub> Laminates with 4 nm Thickness*

AFM images of the layers are presented in Figure 4.16. As can be seen from the figure, layers show a surface comparable to the substrate roughness for 320 and 420 °C deposition temperatures. Some features are visible in the laminate deposited at 620 °C. It could be possible that these features are the crystallites that already have been formed at 520 °C, as observed in the TEM images (Figure 4.17).

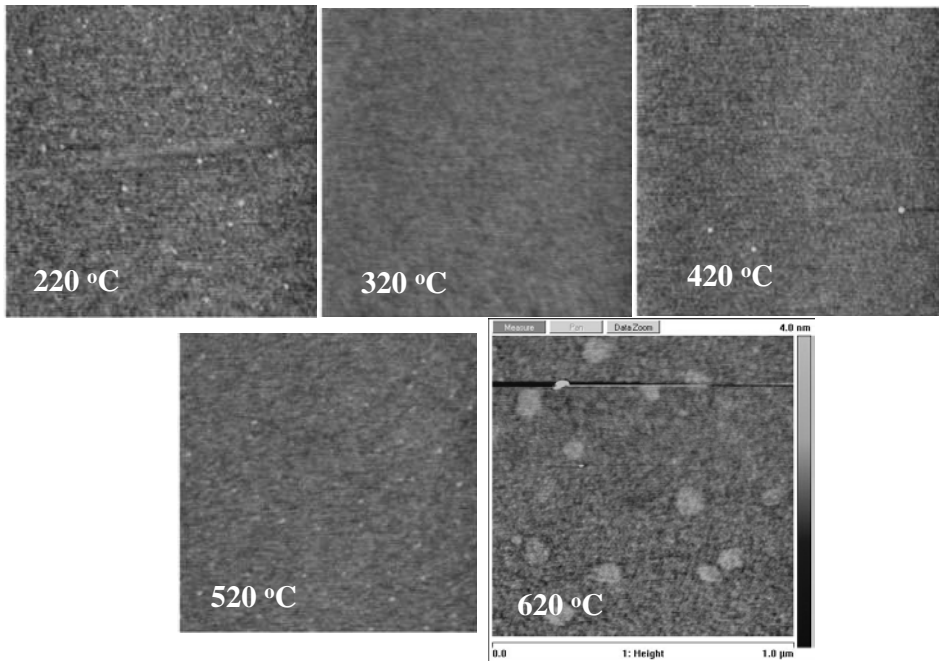
Cross sectional TEM images of the layers are presented in Figure 4.17. The figure shows that the laminate deposited at 420 °C is amorphous, whereas in the layer deposited at 520 °C formation of crystallites is observed. The layer deposited at 850 °C shows clearly a polycrystalline layer, with crystallite sizes of about 4 nm in average. Note the excessive amount of interface oxide in this layer. TEM images show the presence of the laminated structure in films deposited at 420 °C and 520 °C. The crystallites in the laminate deposited at 850 °C, fit to the tetragonal CeHfO<sub>4</sub> structure, as well as cubic CeO<sub>2</sub> and HfO<sub>2</sub>. On the other hand, the crystallites formed in the laminate deposited at 520 °C, where the individual layers are distinguishable, may consist of

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<sup>11</sup> See also Chapter 2, section 2.3.1 for details of substrate pre-treatments.

<sup>12</sup> See Chapter 2 for details of reducing ambient deposition followed by *in-situ* PDA.

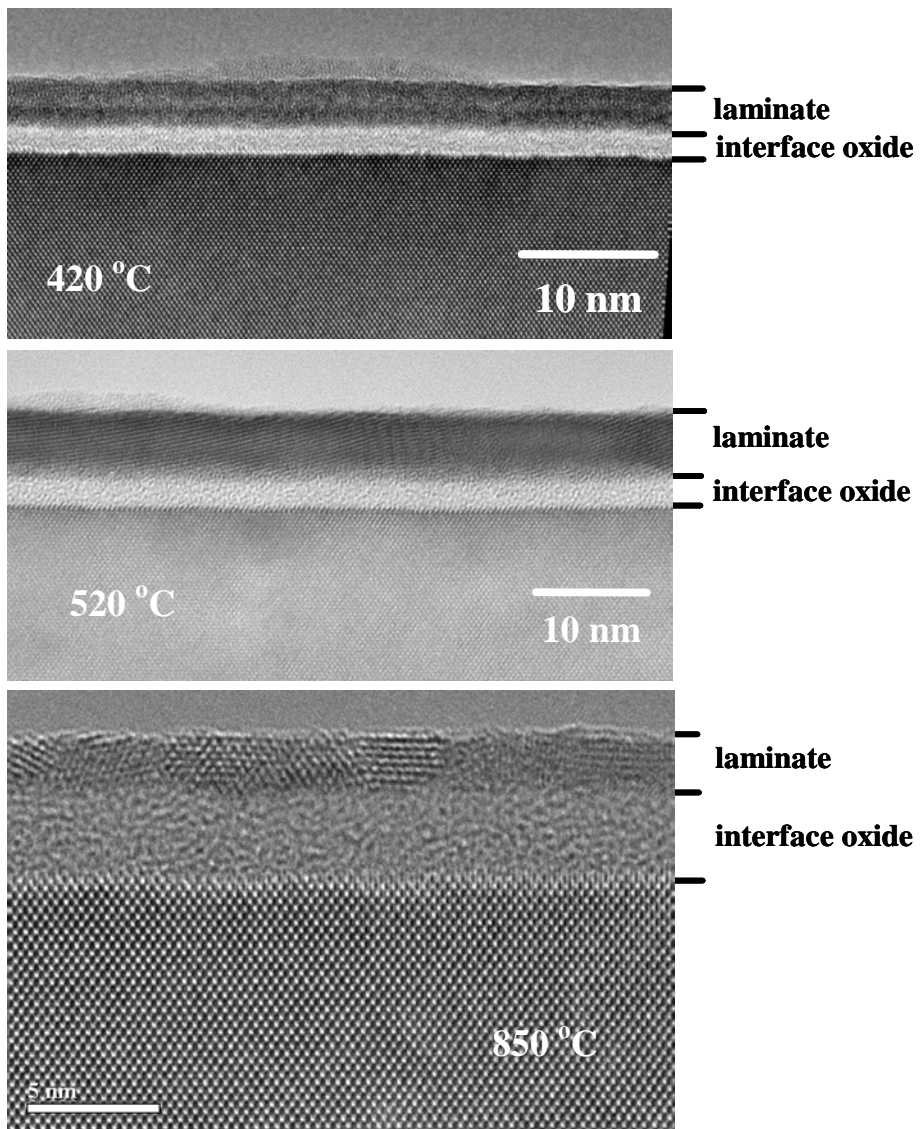
different crystal structures along the growth direction: A possibility is a compositional change from CeO<sub>2</sub> to CeHfO<sub>4</sub> or a cerium enriched HfO<sub>2</sub> in the growth direction.



**Figure 4.16:** AFM images of CeO<sub>2</sub>-HfO<sub>2</sub> laminates 4 nm in thickness, deposited at different temperatures (Image size is 1x1 μm<sup>2</sup> and image depth is 4 nm)

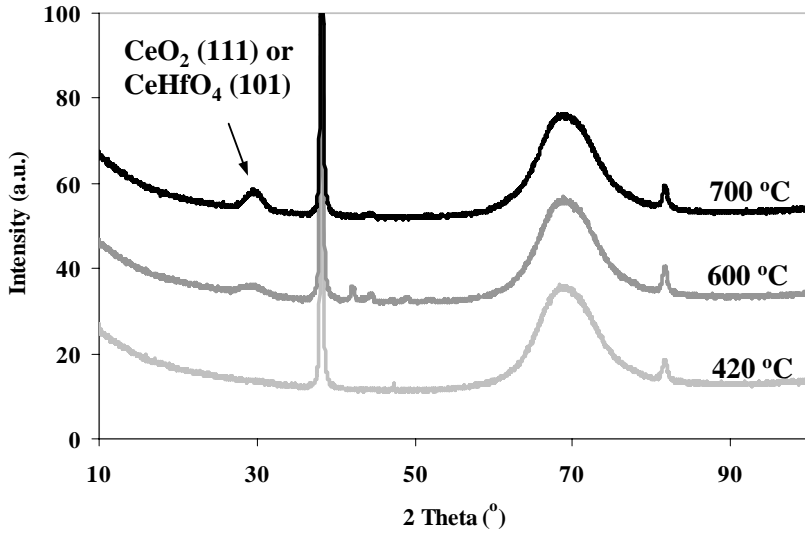
The effect of the deposition temperature on the interface oxide thickness of 2 nm thickness laminates is investigated by XPS and results are presented in Figure 4.19. The interface oxide thickness is found to be higher than those seen in TEM analysis of 4 nm thickness laminates (Figure 4.17). This difference is related with the thickness of the laminate, since the deposited layer thickness has a limiting effect on the oxygen diffusion towards interface during *in-situ* PDA.

XRD analysis of the layers deposited at different temperatures (Figure 4.18) didn't give much information about the exact crystal structure of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates. The peak formed at higher deposition temperatures around 30 ° shows the presence of a crystalline structure but this peak fits CeO<sub>2</sub> (111) and HfO<sub>2</sub> structures, as well as the CeHfO<sub>4</sub> (101).

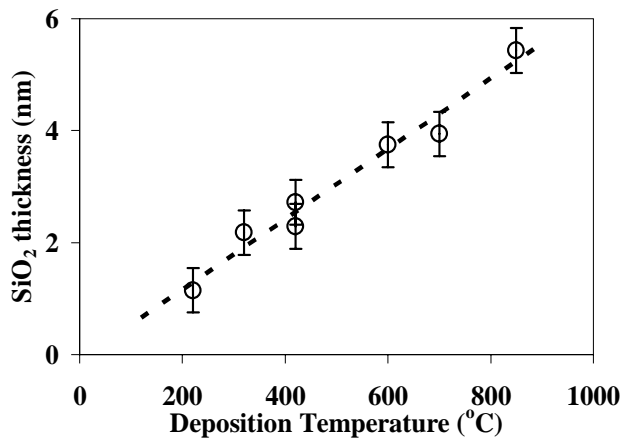


**Figure 4.17:** Cross sectional TEM images of laminates deposited at different temperatures: 420 °C (top), 520 °C (middle) and 850 °C (bottom). Note that, the magnification of the bottom image is higher than others for presenting more details of crystallites.



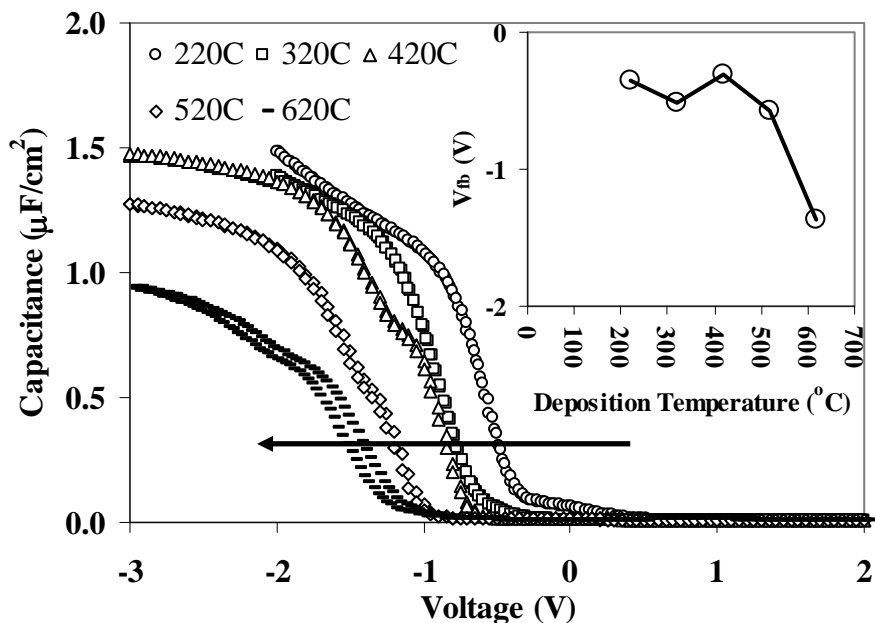


**Figure 4.18:** XRD patterns of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates deposited at different temperatures



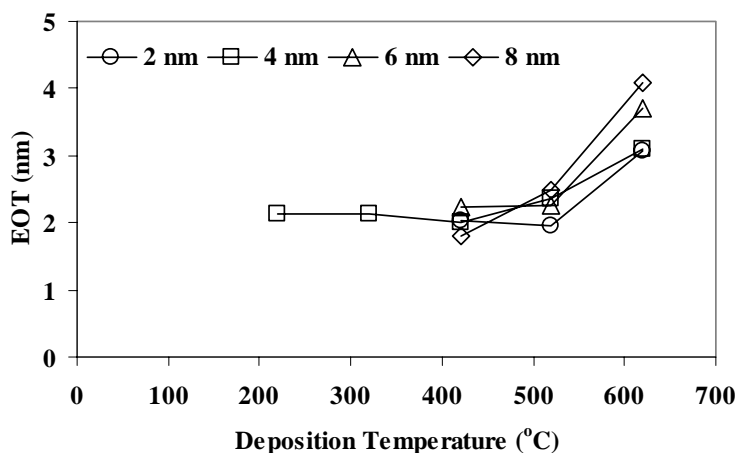
**Figure 4.19:** Effect of deposition temperature on interface oxide thickness of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates 2 nm in thickness, analyzed by XPS.

*C-V* measurements of these laminates are presented in Figure 4.20. As a general tendency in *C-V* plots, an increased hysteresis for higher deposition temperatures is observed. This can be the effect of the crystallization of the layers at elevated temperatures, which is observed in the layers deposited at 520 °C (Figure 4.17) and therefore expected to be more in the layer deposited at 620 °C. However, note the differences in voltage sweep range of *C-V* measurements, *i.e.* different accumulation voltages, may also lead differences in hysteresis. Another feature in the *C-V* plots is the shift in  $V_{fb}$  depending on the deposition temperature to more negative voltages, which indicates less negative charges in the layers grown at elevated temperatures.



**Figure 4.20:**  $C$ - $V$  plots of the  $\text{CeO}_2$ - $\text{HfO}_2$  laminates with 4 nm thicknesses deposited at different temperatures. Inset shows the  $V_{fb}$  of the layers extracted by CVC simulation.

The EOT and  $D_{it}$  values of the layers show two distinct behaviors for deposition temperatures below and above 420  $^{\circ}\text{C}$ . The EOT of the layers, extracted from  $C$ - $V$  measurements, shows an increase above 420  $^{\circ}\text{C}$ , as can be seen from Figure 4.21. The layers deposited below 420  $^{\circ}\text{C}$  have similar EOT values and EOT starts to increase for higher deposition temperatures. This is related to the increased interface oxide thickness for higher deposition temperatures as shown in Figure 4.21.



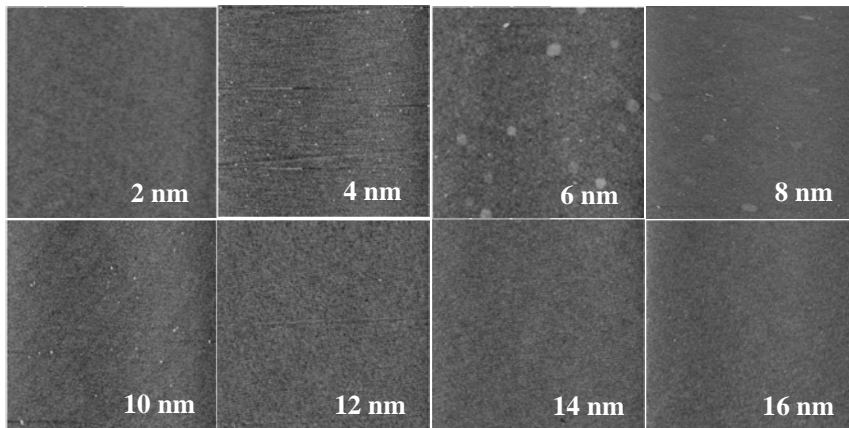
**Figure 4.21:** EOT of the  $\text{CeO}_2$ - $\text{HfO}_2$  laminates with different thicknesses (2 to 8 nm) deposited at different temperatures.

In conclusion, it's found that the electrical and morphological properties found to be changing significantly for deposition temperatures from 420 °C to 620 °C. This change is correlated to the crystallization of the layers with increasing temperature, as well as the effective oxidation during deposition *and* PDA.

#### CeO<sub>2</sub>-HfO<sub>2</sub> Nanolaminates Deposited at 420, 520 and 620 °C

A thickness series from 2 nm to 16 nm of the laminates were deposited at 420 °C and 520 °C and compared to an additional thickness series of laminates deposited at 620 °C with a thickness range of 2 to 8 nm. Layers are deposited at 0.1 mbar Ar+H<sub>2</sub>, followed by an *in-situ* PDA with a 5 °C/min cooling rate. MOS devices with TaN electrodes were prepared with 420 and 520 °C deposited laminated dielectrics. For the laminates deposited at 620 °C the gate metal was Au, deposited by sputtering via a shadow mask

The main interest was the earlier mentioned transition of the properties of the laminates from 420 °C and 520 °C deposition temperatures. The electrical and structural properties of the laminates are characterized and the properties are compared with each other, as well as with the single CeO<sub>2</sub> and HfO<sub>2</sub> reference layers<sup>13</sup> deposited at 420 and 520 °C.

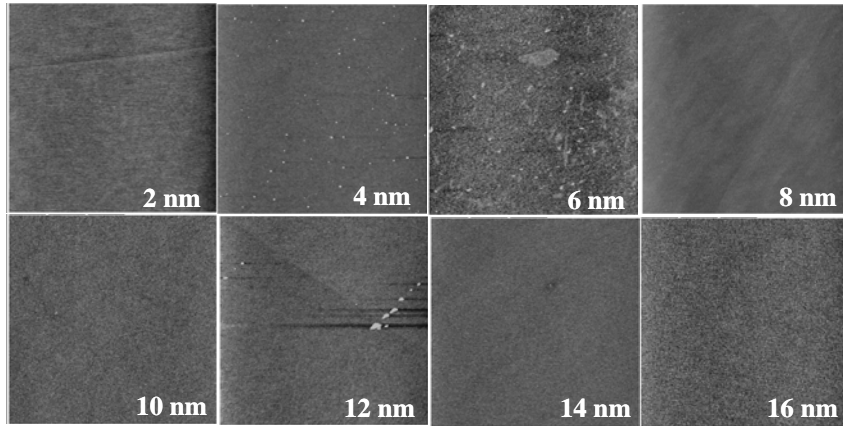


**Figure 4.22:** AFM images of the CeO<sub>2</sub>-HfO<sub>2</sub> nanolaminates with thicknesses from 2 nm to 16 nm deposited at 420 °C. Image size is 2 x 2 μm<sup>2</sup> and image depth scale is 4 nm.

AFM images of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates, with thickness from 2 nm to 16 nm, deposited at 420 °C are presented in Figure 4.22. Images show that crystallization in the laminates starts at 6 nm and crystallites formed in the layer appears as islands in the images. A better comparison about crystallite formation can be done by comparing that

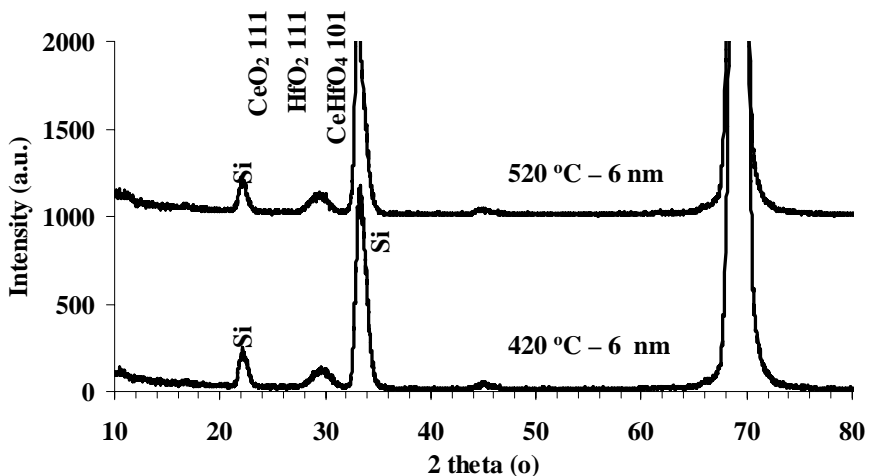
<sup>13</sup> See Chapter 3 for the detailed analyses of CeO<sub>2</sub> and HfO<sub>2</sub> reference layers.

image with the AFM image of 620 °C deposited laminate shown in Figure 4.17. Laminates with thicknesses above 8 nm, shows a smooth surface, which may indicate a homogeneous structure.



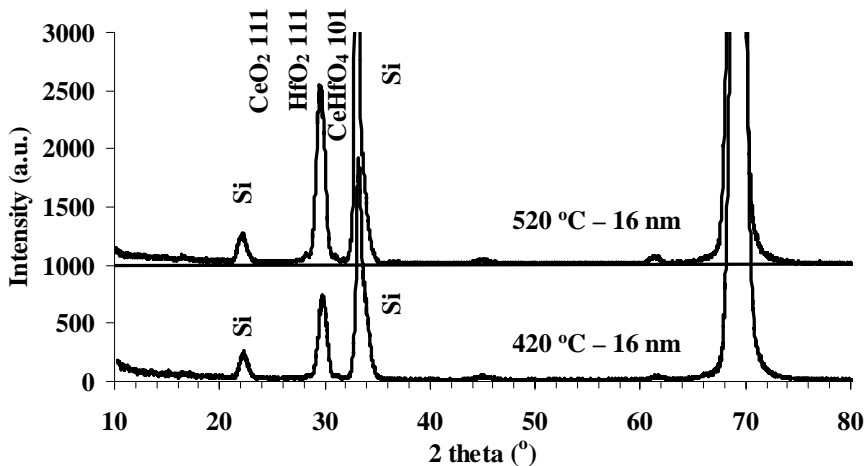
**Figure 4.23:** AFM images of the CeO<sub>2</sub>-HfO<sub>2</sub> nanolaminates with thicknesses from 2 nm to 16 nm deposited at 520 °C. Image size is 2 x 2 μm<sup>2</sup> and image depth scale is 4 nm.

CeO<sub>2</sub>-HfO<sub>2</sub> nanolaminates deposited at 520 °C also have some features in 6 nm layer as presented in AFM images in Figure 4.23. Despite the 420 °C deposition temperature, the 6 nm layer deposited at 520 °C have some acicular (needle-like) features in AFM image besides round shape ones. The origin of these acicular features is not known.



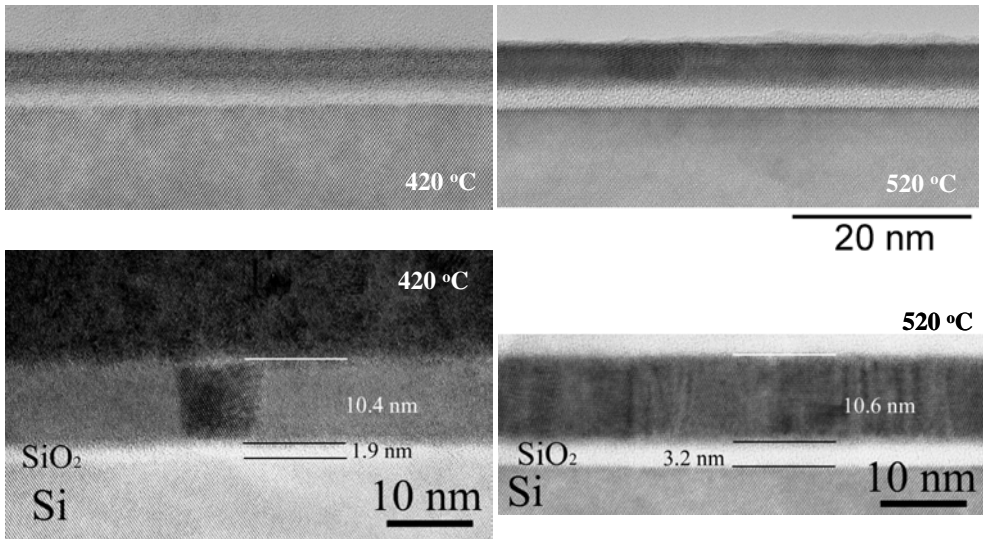
**Figure 4.24:** XRD patterns of the 6 nm laminates deposited at 420 °C (bottom) and 520 °C (top).

A possible change in the morphology of the laminates, deposited at 420 and 520 °C, with increasing thickness is investigated by XRD and TEM analyses. Figure 4.24 and 4.25, shows the XRD patterns of 420 and 520 °C deposited laminates of 6 nm and 16 nm layers, respectively. FWHM of the peak, located around 29.8 ° corresponds to possible phases in the CeO<sub>2</sub>-HfO<sub>2</sub> laminated structure is indicating that the crystallinity of the 16 nm laminates is quite higher for both deposition temperatures, compared to the 6 nm laminates

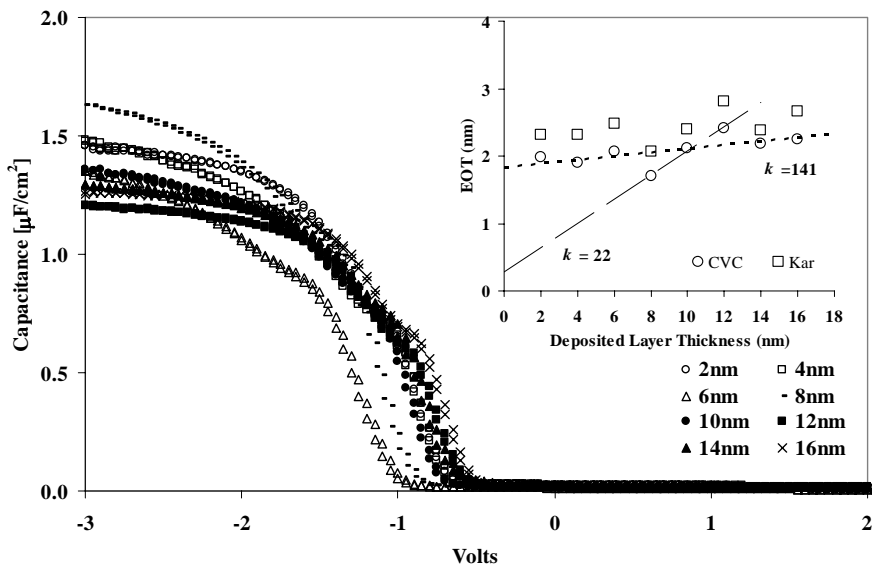


**Figure 4.25:** XRD patterns of the 16 nm laminates deposited at 420 °C (bottom) and 520 °C (top).

Figure 4.26 shows the cross sectional TEM images of the laminates deposited at 420 and 520 °C. The deposited layer thickness estimation of the laminates was 4 nm for thin layers and 16 nm for thick layers presented in the figure. For 4 nm deposited thickness layers, TEM images are consistent with the deposited layer thickness estimation. However, the thicknesses of the layers with 16 nm layer thickness estimation, according to the TEM images, are found thinner. This difference between the estimated thickness and the actual one is believed to be the result of the calibration the deposition rate, which was performed on the amorphous layers. As can be seen from the figure, layers, with 16 nm estimated thickness, are crystalline for both deposition temperatures; hence the difference of thickness can be the result of densification of the layers during transition from amorphous phase to the crystalline. The laminated structure is visible in the 4 nm layers for both deposition temperatures, whereas the 16 nm layers have a homogeneous, polycrystalline structure instead of an amorphous laminated one.



**Figure 4.26:** Cross sectional TEM images of the laminates deposited at 420 °C (left) and 520 °C (right) with 4 nm (top) and 16 nm (bottom) deposited thicknesses.



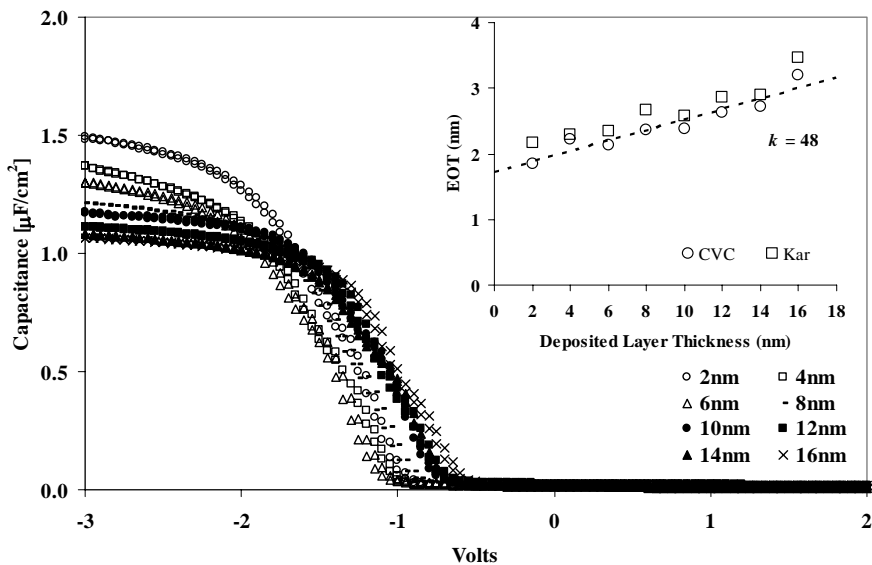
**Figure 4.27:** C-V plots of the CeO<sub>2</sub>-HfO<sub>2</sub> nanolaminates deposited at 420 °C. Inset shows the EOT (extracted by CVC simulation and the Kar method) vs. thickness and dashed lines are the linear fits.

C-V plots of the laminates deposited at 420, 520 and 620 °C and their EOT values are presented in figures 4.27, 4.28 and 4.29, respectively. It's found that layers deposited at 420 °C have an unexpectedly high dielectric constant of 141 according to the calculation based on the slope of the linear fit of EOT-thickness data. This behavior,

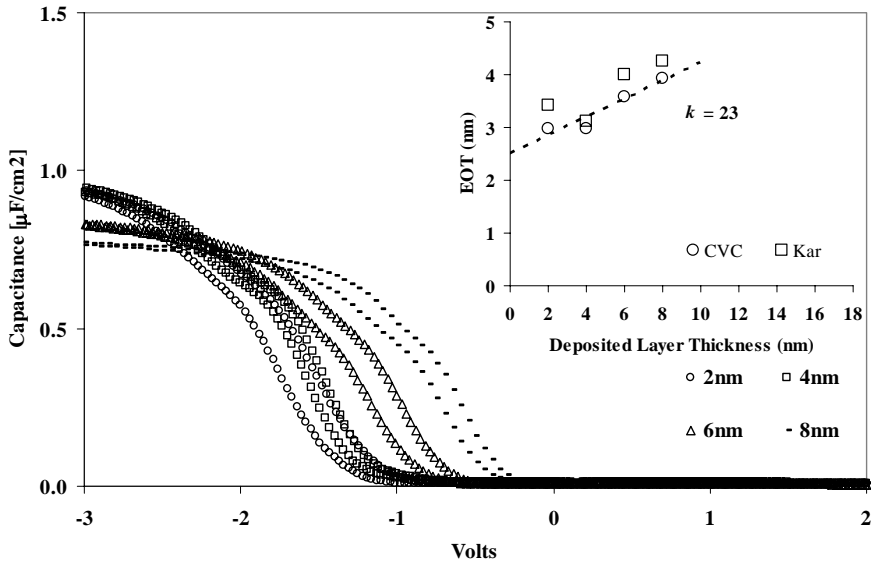
similar to CeO<sub>2</sub> reference layers deposited at same temperature (see Chapter 3), is a result of the thickness dependency of the laminates. As the thinner layers remain amorphous, the thicker layers tend to crystallize and the properties of the dielectric change for different morphologies.

The other part of the thickness depending behavior is originated from *in-situ* high pressure oxygen post deposition annealing: For a given deposition temperature and cooling rate, the amount of oxygen diffused to the interface is decreasing with increasing layer thickness. Therefore, thinner layers are expected to form a thicker interface due to excessive oxidation, and as the deposited layer thickness increases, a decrease in the interface oxide thickness is therefore expected. The secondary linear fit of the EOT plot of 420 °C deposited laminates in Figure 4.30, which gives a *k* value of 23, also shows the result of mentioned thickness dependency of the layer morphology.

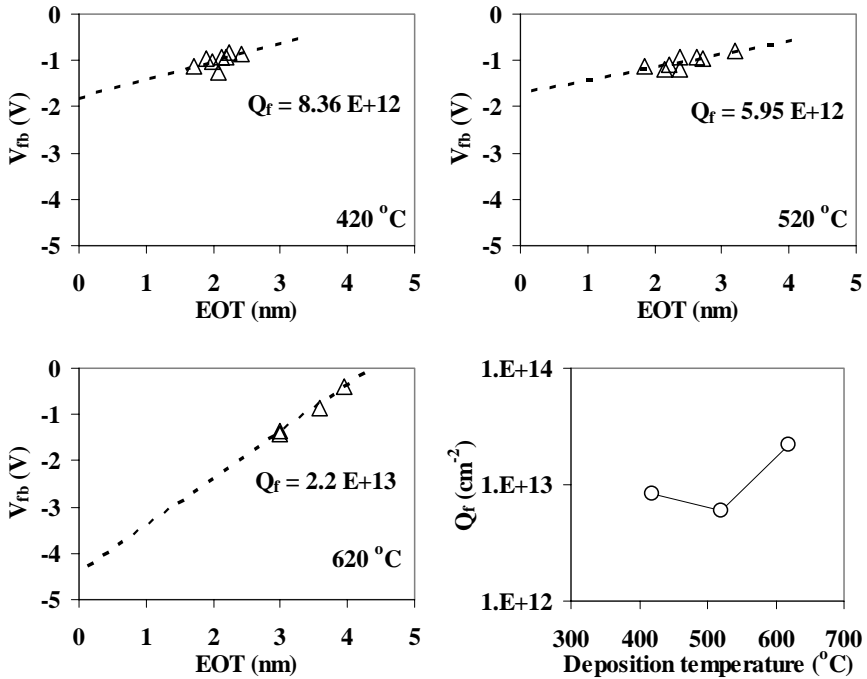
*C-V* plots also shows an increased hysteresis for high deposition temperature, which reaches up to 200 mV for the layers deposited at 620 °C, whereas the layers deposited at 420 and 520 °C have a hysteresis less than 50 mV.



**Figure 4.28:** *C-V* plot of the CeO<sub>2</sub>-HfO<sub>2</sub> nanolaminates deposited at 520 °C. Inset shows the EOT (extracted by CVC simulation and Kar method) vs. thickness and dashed line is the linear fit.



**Figure 4.29:** C-V plot of the  $\text{CeO}_2\text{-HfO}_2$  nanolaminates deposited at  $620^\circ\text{C}$ . Inset shows the EOT (extracted by CVC simulation and Kar method) vs. thickness and dashed line is the linear fit.

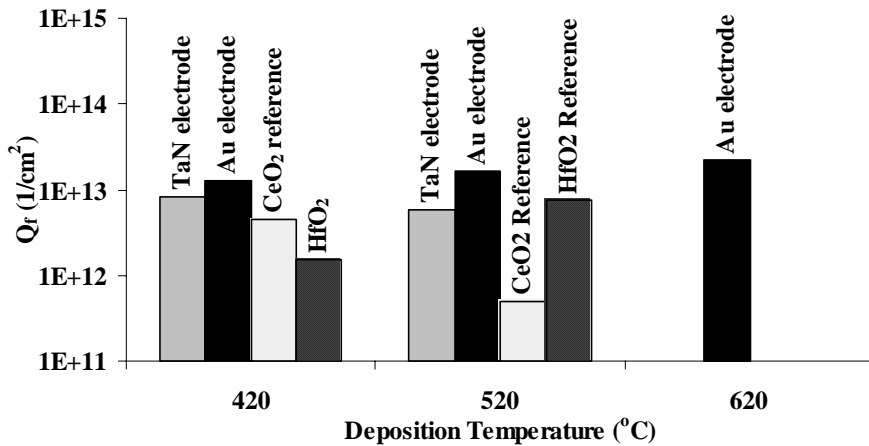


**Figure 4.30:**  $V_{fb}$ -EOT plots of the  $\text{CeO}_2\text{-HfO}_2$  laminates deposited at different temperatures. Their  $Q_f$  values extracted from the slope of  $V_{fb}$ -EOT plot's linear fit, is also presented as a function of deposition temperature.



The  $V_{fb}$  of the laminates extracted by CVC are presented in Figure 4.30, as well as their  $Q_f$  values extracted from the slope of the linear fit of  $V_{fb}$ -EOT plots. As a first aspect, intersection of the linear fit, which gives the work function difference of the electrodes on silicon, is different for the layers deposited at 620 °C.

As mentioned earlier in this section, the electrode of the MOS devices for 620 °C laminates is Au, whereas the other laminates deposited at 420 and 520 °C have a TaN electrode, which results in two different  $\phi_{ms}$ . However, a different set of layers prepared with gold layers for 420 and 520 °C deposition temperatures, also shows higher  $Q_f$  than the TaN electrode ones. Figure 4.31 shows the  $Q_f$  values, extracted from  $V_{fb}$ -EOT plots, for TaN and Au electrodes, as well as the  $Q_f$  values of the CeO<sub>2</sub> and HfO<sub>2</sub> reference layers. Although the measurement data quality from the MOS devices of the layers deposited at 420 and 520 °C with Au electrodes were lower<sup>14</sup> than those with TaN electrodes, it's remarkable that the  $Q_f$  of the laminates with Au electrode is found to be higher than laminates with TaN electrode.

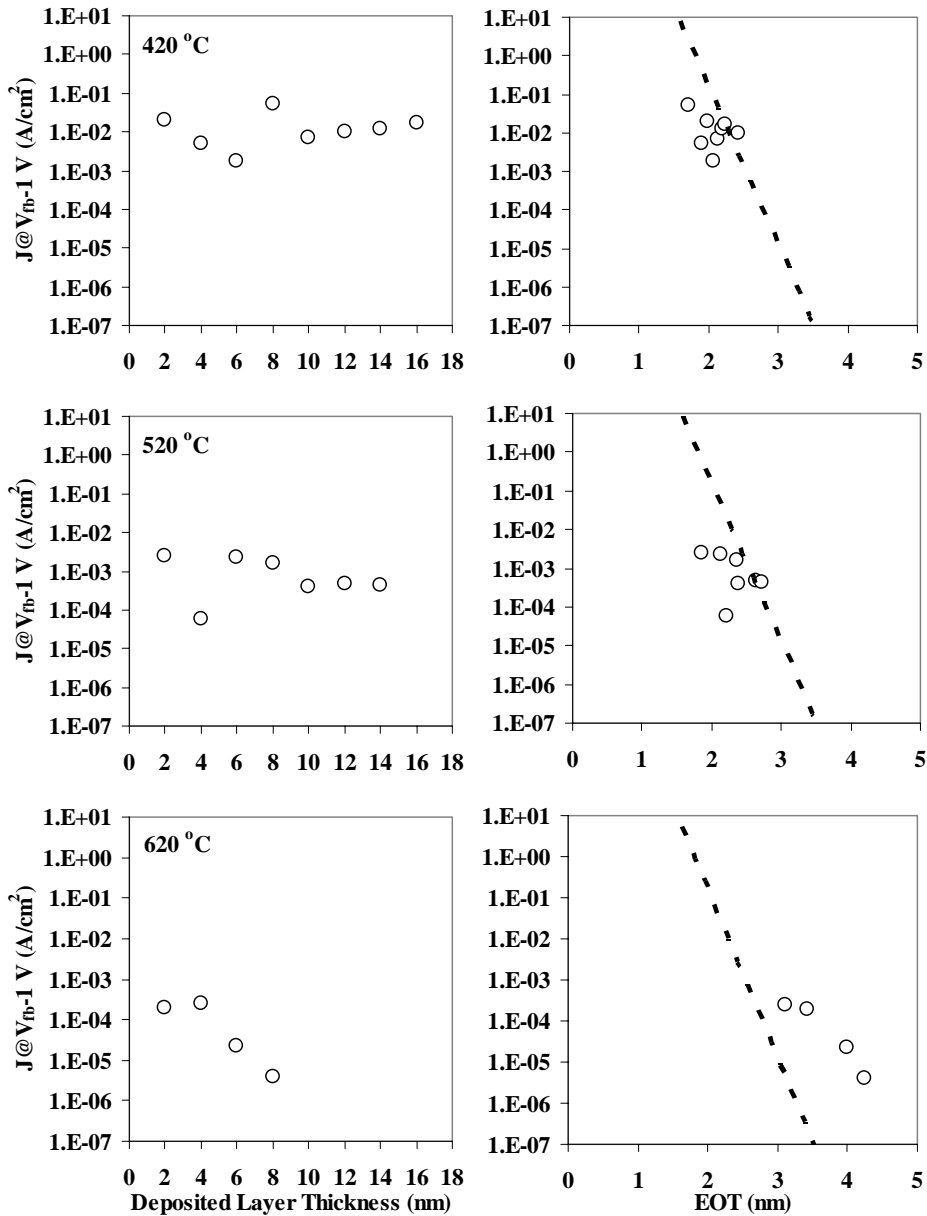


**Figure 4.31:**  $Q_f$  values of the laminates deposited at different temperatures and with different electrodes (Au and TaN), compared with CeO<sub>2</sub> and HfO<sub>2</sub> reference layers.

Leakage current densities of the laminates with different deposition temperatures are presented in Figure 4.32. As a general trend, leakage current density decreases with the increasing temperature as observed in  $J$ -EOT plots. However,  $J_g$  doesn't show a continuous reduction with physical thickness. For instance, there are two main trends in leakage current density with increasing physical thickness for the laminates deposited at 420 and 520 °C: For thinner layers (up to 4, 6 nm) a reduction is observed and thicker layers (above 6 nm) didn't follow that trend. However, the laminates deposited at 620 °C show a reduction in leakage current density with

<sup>14</sup> Scattering of the data of the devices with Au electrode along the linear fit was considerably more than those with TaN electrode.

increasing thickness. This difference in leakage current reduction trends of different deposition temperatures is correlated to the morphological changes (*i.e.* transformation from amorphous to crystalline) of the laminates with increasing thickness, as already shown by TEM and XRD analyses.



**Figure 4.32:**  $J_g$  vs. deposited layer thickness (left) and EOT (right), measured at  $V_{fb}-1 V$ , of the  $\text{CeO}_2\text{-HfO}_2$  laminates deposited at different temperatures. Dashed lines are  $\text{SiO}_2$  reference data.

The difference of interface oxide formation during deposition and/or *in-situ* oxygen PDA may also affect the leakage current characteristics. Increased deposition temperature increases the interface oxide thickness as shown in Figure 4.18. Effect of *in-situ* PDA is the result of two possible mechanisms depending on oxygen diffusion: A more stabilized interface oxide formation by means of more oxygen diffusion at high temperatures, *and* decreasing the oxygen vacancies in the laminates by means of more effective oxidation. In first case, PDA creates thicker (or more stabilized) interface oxides for thinner layers, where the oxygen diffusion to the interface region is relatively higher. In latter case, oxidation of the layers may not be completed for the whole thickness range of thicker layers; hence, increased amount of oxygen vacancies may result in the observed difference in leakage current reduction trends between thinner and thicker layers.

In conclusion, the amorphous laminates show significantly better leakage current characteristics than the polycrystalline ones. It's also been observed that the crystallinity of the layers depends on the physical thickness, as well as the deposition temperature. Effect of the thickness dependency of the layers is found to be more for lower deposition temperatures.

#### 4.5. Effect of the Cooling Rate During *in-situ* PDA

Cooling rate during *in-situ* high pressure oxygen PDA determines the time that the layer is exposed to oxygen at high temperatures. In that manner, one should expect several major effects of the cooling rate on the layer characteristics:

- Changes the oxidation state of the layer (lower cooling rates results in better oxidation).
- Changes the interface oxide thickness and/or composition.
- Changes the crystallinity of the layer (lower cooling rates results in high crystallinity).

The properties of the layers with 5 °C/min cooling rate were already discussed in the previous section of this chapter. The layers annealed with a cooling rate of 2 and 10 °C/min are presented in this section, and their properties are compared to each other and to the CeO<sub>2</sub> reference layers.

##### 4.5.1. Experimental

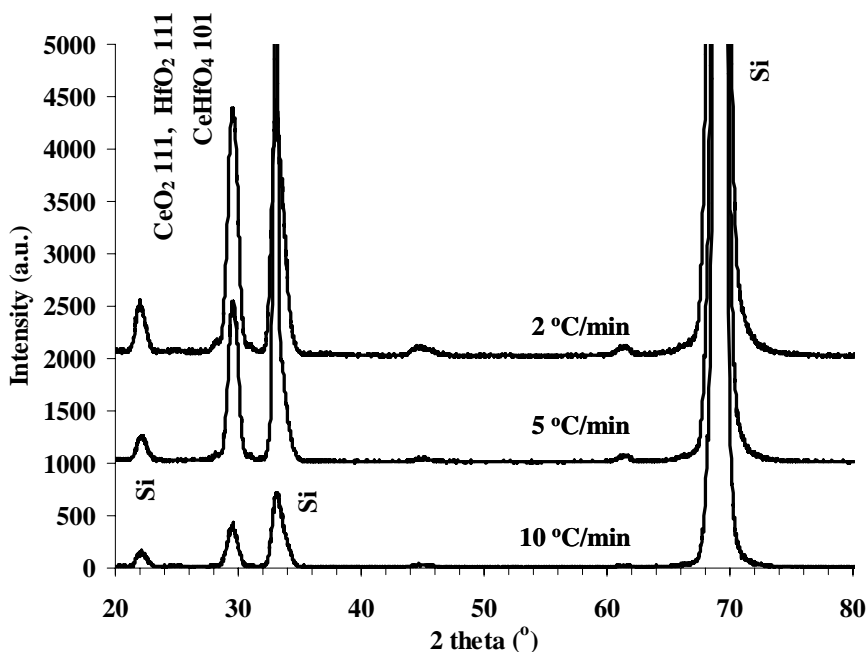
CeO<sub>2</sub>-HfO<sub>2</sub> laminated structures<sup>15</sup> with different thicknesses up to 16 nm are deposited in 0.1 mbar Ar+H<sub>2</sub> at 520 °C on hydrogen passivated Si substrates. Three

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<sup>15</sup> Laminates were in C-H-C-H sequence, with an individual layer thickness of 1 nm.

different cooling rates of 2, 5 and 10 °C/min are applied during in-situ high pressure ( $p_{O_2}=100$  mbar) oxygen PDA<sup>16</sup>.

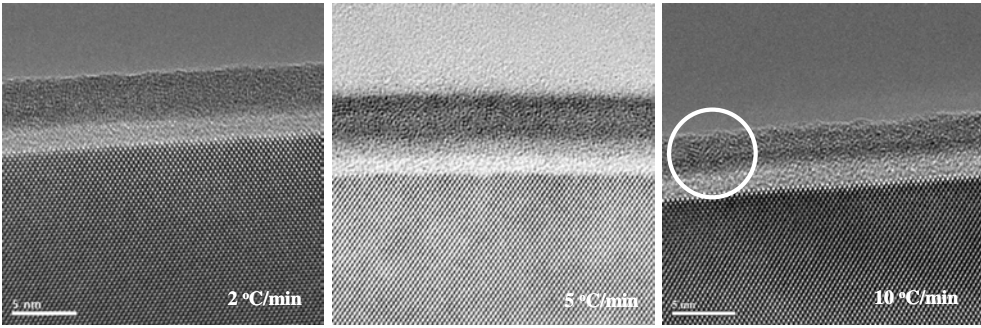
XRD patterns of the 16 nm laminates for three different cooling rates (Figure 4.33) show that the crystallinity of the layers are strongly affected by their cooling rates. 10 °C/min cooling rate gives the lowest crystallinity and the crystallinity increase with the decreasing cooling rate. However, the cross sectional TEM images of 4 nm layers presented in Figure 4.34, shows that the layers are amorphous and laminated structure is visible in the layers. This behavior agrees with the thickness dependency of the crystallinity, as shown in the previous section of this chapter, where the effects of deposition temperature are discussed.



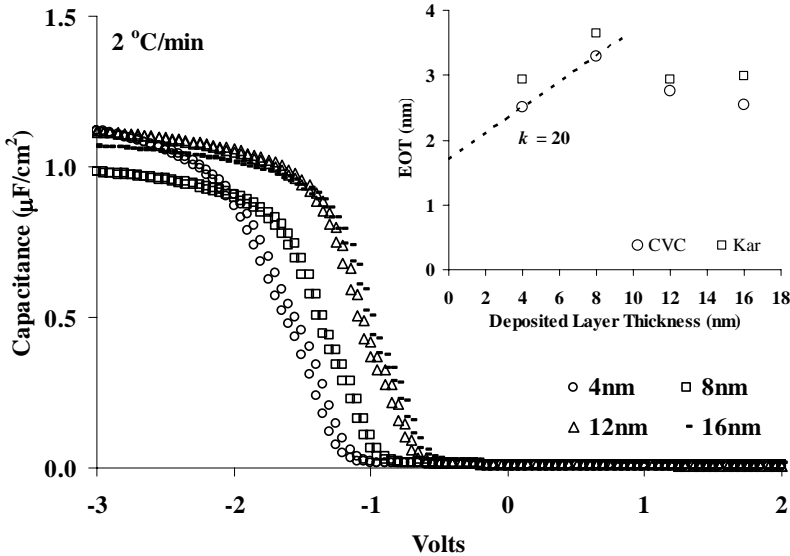
**Figure 4.33:** XRD patterns of the 16 nm layers with 2, 5 and 10 °C/min cooling rates.

Electrical characterization of the layers is performed with the MOS devices with TaN electrodes. *C-V* plots and the EOT values extracted from them, of the different thicknesses of the layers with 2 and 10 °C/min cooling rates are shown in Figures 4.35 and 4.36, respectively. *C-V* plots of the 4 nm layers, for all cooling rates, have more hysteresis compared to the thicker layers, which indicates more trapped charge in thinner layers.

<sup>16</sup>See Chapter 2 for details of the PDA process.

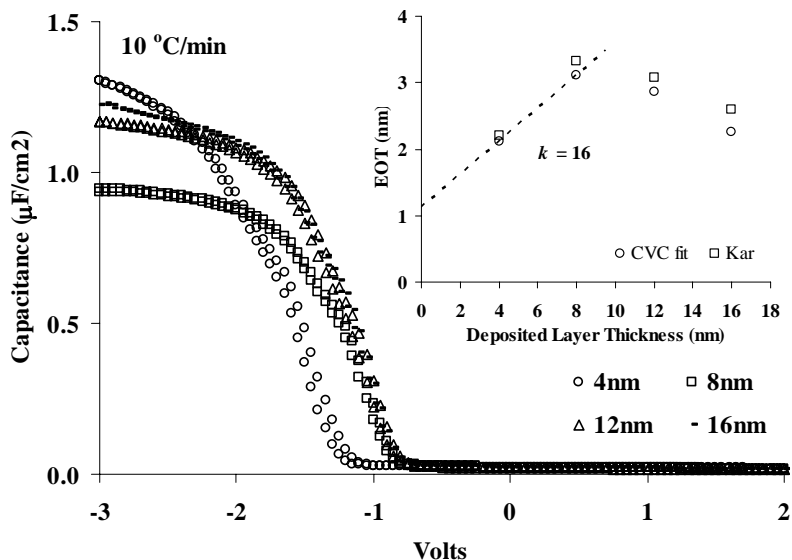


**Figure 4.34:** TEM images of the 4 nm laminates with three different cooling rates. The encircled area shows a crystalline-like formation in the layer with a cooling rate of 10 °C/min. Scale bar in the images is 5 nm.

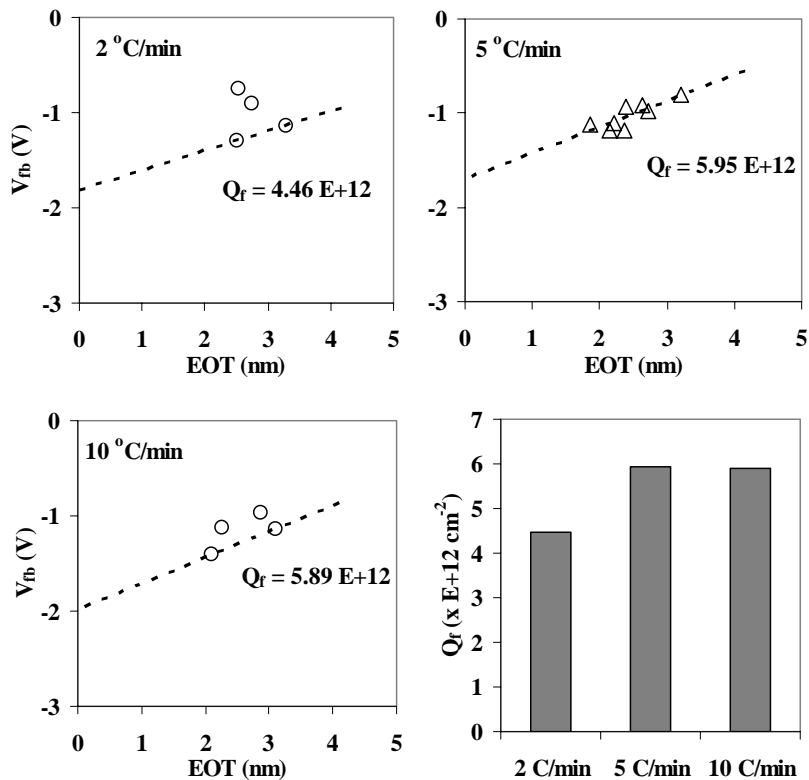


**Figure 4.35:** C-V plots of the 4 to 16 nm layers with a cooling rate of 2 °C/min. Inset shows the EOT values extracted from C-V plots by CVC simulation and the Kar method.

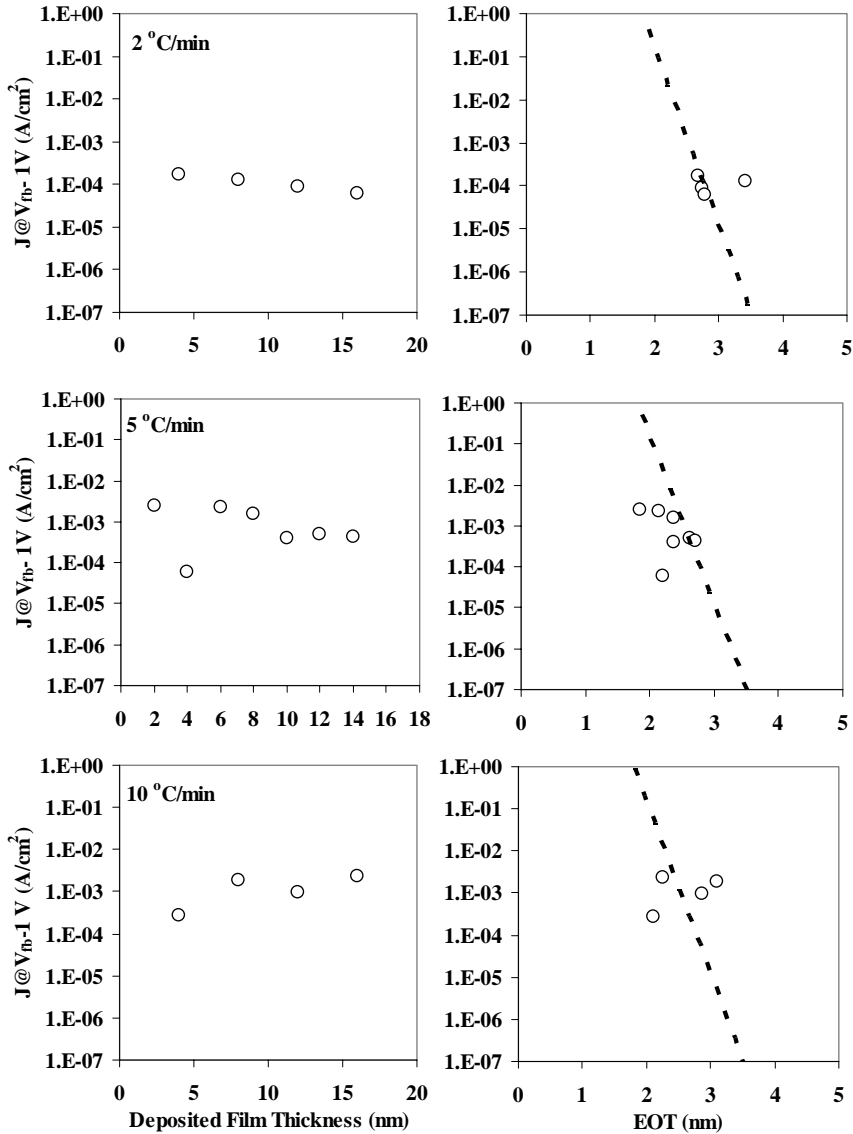
An important result from the C-V analyses is the different EOT vs. deposited layer thickness trends for different cooling rates: As can be seen from the figures, EOT doesn't increase for the increased physical thickness for 12 and 16 nm layer thicknesses. The EOT tends to decrease for these thicknesses, contrary to the ones with a cooling rate of a 5 °C/min (see Figure 4.28). This is also correlated to the thickness dependency of the EOT of the laminates, as described in previous chapters. Effect of the interface oxide formation is more dominant for the laminates with 2 °C/min cooling rate, whereas the effect of crystallization is more dominant for the laminates with 10 °C/min cooling rate. Both effects are seemed to be balanced for the intermediate cooling rate of a 5 °C/min.



**Figure 4.36:** C-V plots of the 4 to 16 nm layers with a cooling rate of 10 °C/min. Inset shows the EOT values extracted from C-V plots by CVC simulation and the Kar method.



**Figure 4.37:**  $V_{fb}$ -EOT of the laminates with 2, 5 and 10 °C/min cooling rates. Their  $Q_f$  values extracted from the slopes of the linear fits are presented as well (bottom right).



**Figure 4.38:**  $J_g$  at  $V_{fb-1} V$  of the layers with different cooling rates during PDA, presented as the function of the deposited layer thickness (left) and EOT (right). Dashed lines are SiO<sub>2</sub> reference data.

$V_{fb}$ -EOT of the laminates, which are presented in Figure 4.37, also shows significant differences for different cooling rates. Since the EOT of the layers with 2 and 10 °C/min cooling rates is following a different trend for 12 and 16 nm thicknesses, only the EOT and  $V_{fb}$  values belongs to 4 and 8 nm layers are used for  $Q_f$  calculation. The lowest  $Q_f$  ( $Q_f=4.46 \times 10^{12} \text{ cm}^{-2}$ ) is found for 2 °C/min cooling rate, whereas the layers with 5 and 10 °C/min cooling rates have similar  $Q_f$  values,  $Q_f=5.95 \times 10^{12} \text{ cm}^{-2}$  and  $Q_f=5.89 \times 10^{12} \text{ cm}^{-2}$ , respectively. The intersection of the linear fits in the figure

shows a  $\phi_{\text{ms}}$  for the TaN electrode of 1.82, 1.7 and 1.99 eV for 2, 5 and 10 °C/min cooling rates, respectively.

The leakage current characteristics of the laminates with different cooling rates are compared in Figure 4.38. Figure shows that layers with 2 and 10 °C/min cooling rates have no leakage current reduction with the increased physical thickness, whereas the 5 °C/min layers shows a decrease for 2 and 4 nm layers. Leakage current reduction by EOT of the 2 and 10 °C/min cooling rates are also found similar to their physical thickness trends. This can also be explained by the change in layer morphology in thicker layers, as mentioned previously in this chapter.

In conclusion, different cooling rates during PDA showed more clearly the thickness dependent change in the properties of the CeO<sub>2</sub>-HfO<sub>2</sub> laminates. In lower cooling rates (2 °C/min), the effect of interface oxidation seemed to be more dominant on the properties. In higher cooling rates (10 °C/min), change in the layer crystallinity becomes more dominant on the change of the properties of the layers. Both effects seemed to be balanced for a moderate cooling rate of a 5 °C/min.

#### 4.6. Effect of the Oxidation Time During *in-situ* PDA

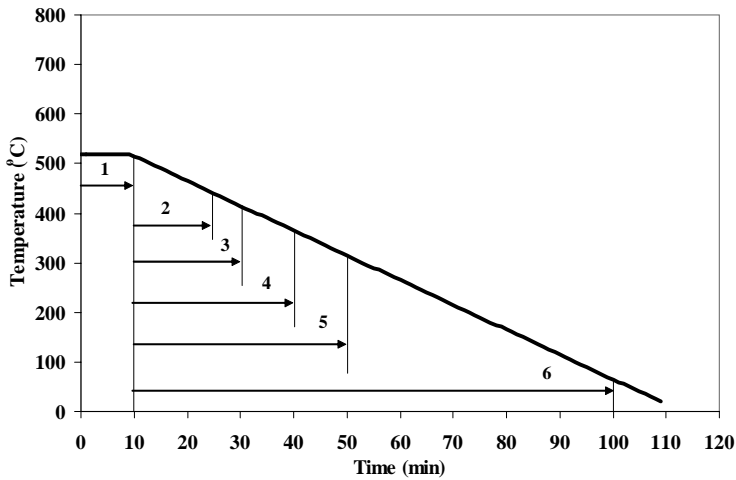
Another way of varying the oxidation level of the layers is changing the time of *in-situ* oxygen PDA, without changing the cooling rate. By keeping the cooling rate constant, the other parameters related to that, *i.e.* crystallinity and the stress level in the film are kept constant as well. Changing the time of PDA is performed by introducing oxygen to the chamber at the start of cooling down and then the oxygen is pumped away after a certain time.

The thicknesses of the layers are also kept constant, to avoid the change in properties as described in the previous sections. A set of experiments was designed to monitor the effect of oxidation time on the CeO<sub>2</sub>-HfO<sub>2</sub> laminated dielectrics with the same thicknesses, and their properties are compared.

##### 4.6.1. Experimental

12 nm CeO<sub>2</sub>-HfO<sub>2</sub> laminates with a C-H-C-H sequence with an individual layer thickness of 1 nm are deposited at 520 °C in 0.1 mbar Ar+H<sub>2</sub> on hydrogen passivated Si (001) substrates. After deposition, the layers are cooled down to room temperature with a cooling rate of 5 °C/min. 100 mbar oxygen is introduced to the deposition chamber for *in-situ* anneal at the very start of the cooling down procedure, at 520 °C.



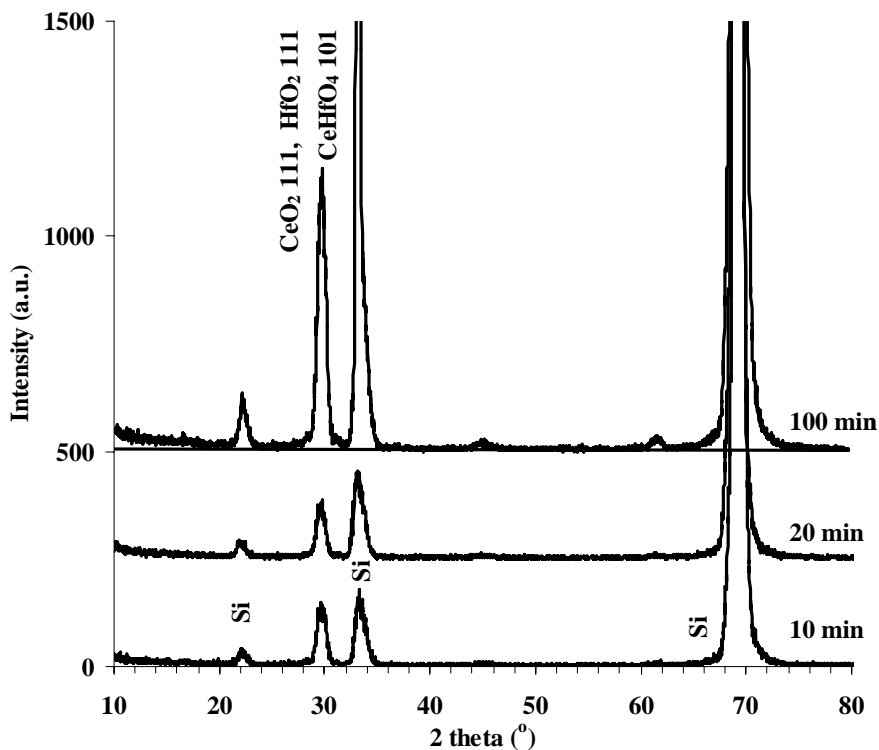


**Figure 4.39:** Time-temperature diagram shows the oxidation times for 6 different layers. Arrows indicate the beginning and the end of oxygen exposure.

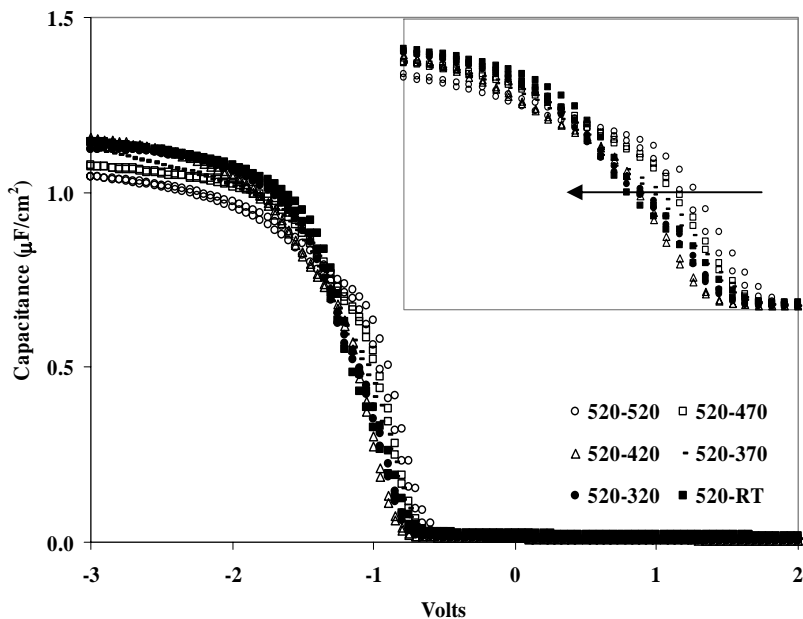
Oxidation time is set by pumping down the oxygen after a certain annealing time during cooling time. Figure 4.39 shows the times and temperatures, where the layers were annealed for different oxidation times. Electrical properties of the layers are characterized by the MOS devices with TaN electrodes. XRD analysis performed for structural characterization.

#### 4.6.2. Results and Discussion

XRD analysis of the layers showed that oxidation time affects the crystallinity of the layers. As can be seen in Figure 4.40, the crystallinity (as a measure of FWHM of the corresponding peak) of the layer exposed to oxygen till room temperature (for 100 minutes) is higher than those have shorter oxidation times. This means that the oxidation has an effect on the crystallinity of the layers; either as decreasing the amount of amorphous phase, or increasing the grain size in the polycrystalline structures. It is difficult to make a conclusion on these two possible effects of oxidation since TEM analysis has not been performed on these layers.



**Figure 4.40:** XRD patterns of the layers oxidized for different periods during cooling down from deposition temperature

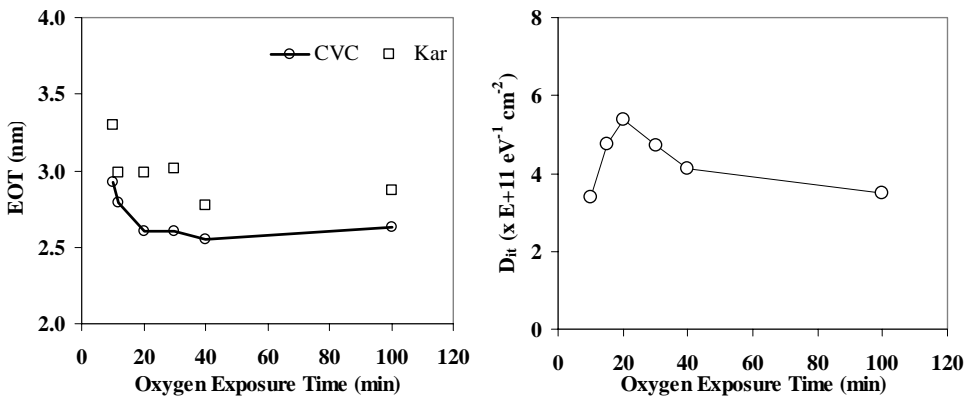


**Figure 4.41:** C-V plots of the layers oxidized for different periods during cooling down from deposition temperature. Inset is the zoomed in view of accumulation region

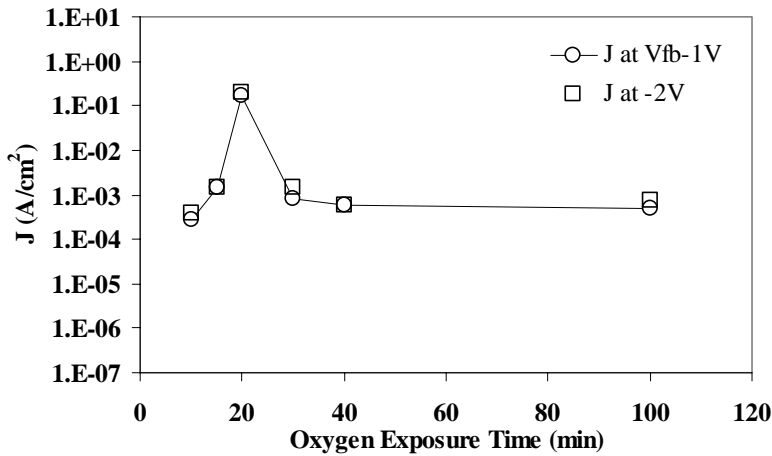
C-V plots of the layers are presented in Figure 4.41. The figure shows that the C-V curves shift to more negative voltages and the width of the shoulder of the C-V plot decreases with increasing oxidation time. This indicates that the oxidation changes the amount of the charges present in the layers and also affects the Si-high-*k* interface characteristics.

Effect of the oxidation time on the  $D_{it}$  and EOT of the layers are shown in Figures 4.42. Figure shows that the EOT of the layers decrease in order of a 0.5 nm by increasing oxidation.  $D_{it}$  values show an increase for the earlier parts of oxidation and then stabilize with increasing oxidation time. This can be correlated to the reaction of oxygen with silicon, during the early stages of oxidation process.

Leakage current densities of the layers (Figure 4.43) shows a similar trend to their  $D_{it}$  plot: Leakage current increases for the early stages of oxidation and then stabilizes with the increased oxidation time. This also indicates that the leakage current properties of the layers are dependent on the interface oxide characteristics. Another aspect that can be concluded from this, may explain when the interface oxide formation begun. As the leakage current density increased by the oxidation time at the initial stages of oxidation, one can say that the interface oxide formed during deposition is destroyed by the diffusion-reaction of oxygen at the silicon interface during annealing. Although the explanation fits to the  $D_{it}$  change for different oxidation times, it also should be noted that a possible formation of crystallites during oxidation may also cause such change in leakage current densities: A polycrystalline structure with smaller grain sizes (and more grain boundaries) for the initial stages of oxidation can evolve a new structure with larger grain sizes (and less grain boundaries) as the oxidation is completed.



**Figure 4.42:** EOT (left) and the  $D_{it}$  (right) of the layers oxidized for different periods as a function of oxidation time.



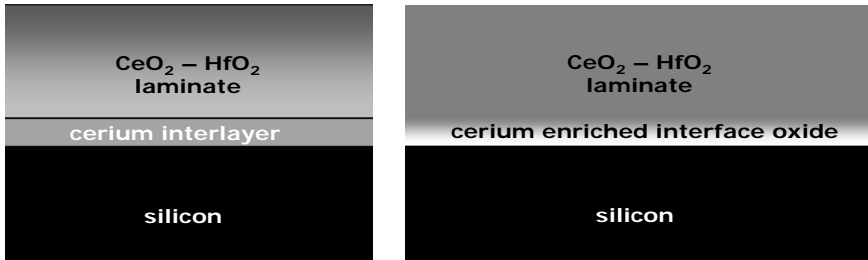
**Figure 4.43:** Leakage current densities of the layers measured at 1 V beyond  $V_{fb}$  and at -2 V, as a function of their oxidation times.

In conclusion, it's found that the early stages of oxygen anneal changes the properties of the interface oxide formed during deposition. As the oxidation time increases, interface oxide stabilizes again.

#### 4.7. Effect of Cerium Metal Interlayer on the Properties of the Nanolaminates

In the previous sections, it is showed that an interface oxide is always formed between silicon and  $\text{CeO}_2\text{-HfO}_2$  laminates. Depositing a thin cerium layer between the silicon substrate and high- $k$  layer is thought to improve the interface oxide characteristics, *i.e.* a decrease in the thickness and/or an increase in the dielectric constant, both, eventually decreases the EOT of the interface oxide. Oxidation of the cerium metal interlayer may occur during deposition and/or during the *in-situ* oxygen PDA. However, depositing a metal layer on top of silicon brings the risk of silicide formation at the interface. Thermodynamic studies of the metal oxides on silicon is showed that cerium oxide (both,  $\text{CeO}_2$  and  $\text{Ce}_2\text{O}_3$ ) is more stable than its silicide, therefore can be used as an 'oxygen gathering' layer. The interface oxide formed with the presence of a cerium metal layer is expected to be a mixture of cerium and silicon oxides [54], which have a higher dielectric constant than silicon oxide.

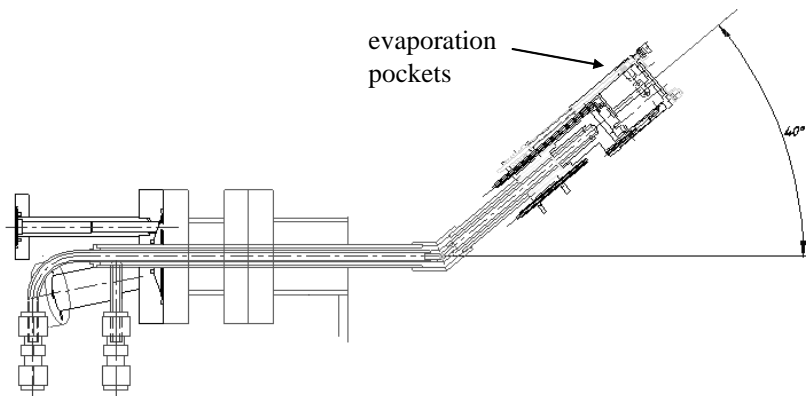
Modification of the Si- $\text{CeO}_2$  interface by depositing a cerium metal layer on top of silicon is investigated in this section. The effect of the e-beam evaporated cerium interlayer (Figure 4.44) on interface oxide thickness, interface state densities and the other properties of the dielectric layer were the main interest of this section.



**Figure 4.44:** Schematic illustration of the cerium metal interlayer deposited between silicon and the CeO<sub>2</sub>-HfO<sub>2</sub> laminate (left) and the final structure after oxidation (right).

#### 4.7.1. Experimental

A cerium metal<sup>17</sup> layer on top of silicon surface is deposited *in-situ* prior to the deposition of CeO<sub>2</sub>-HfO<sub>2</sub> laminates with an e-beam evaporator was specially designed for the PLD chamber (Figure 4.45). Evaporator makes an angle of 40° to the substrate surface normal and the distance to the substrate is set to 40 mm during deposition. Deposition is performed at 10<sup>-7</sup> mbar vacuum and with an ion flux<sup>18</sup> of 3 nA at evaporation pocket<sup>19</sup>. These settings give a deposition rate of a 0.3 nm/min for cerium. The estimated thickness of the cerium layer was 2 monolayers for each deposition.



**Figure 4.45:** Custom designed e-beam evaporator used for *in-situ* evaporation of cerium metal interlayer

Two different thickness series of the laminates from 4 to 16 nm, with a C-H-C-H sequence and an individual layer thickness of 1 nm, are deposited at 520 °C with the

<sup>17</sup> Purity of the cerium metal (granules with diameter of 0.4 mm) was 99.99%.

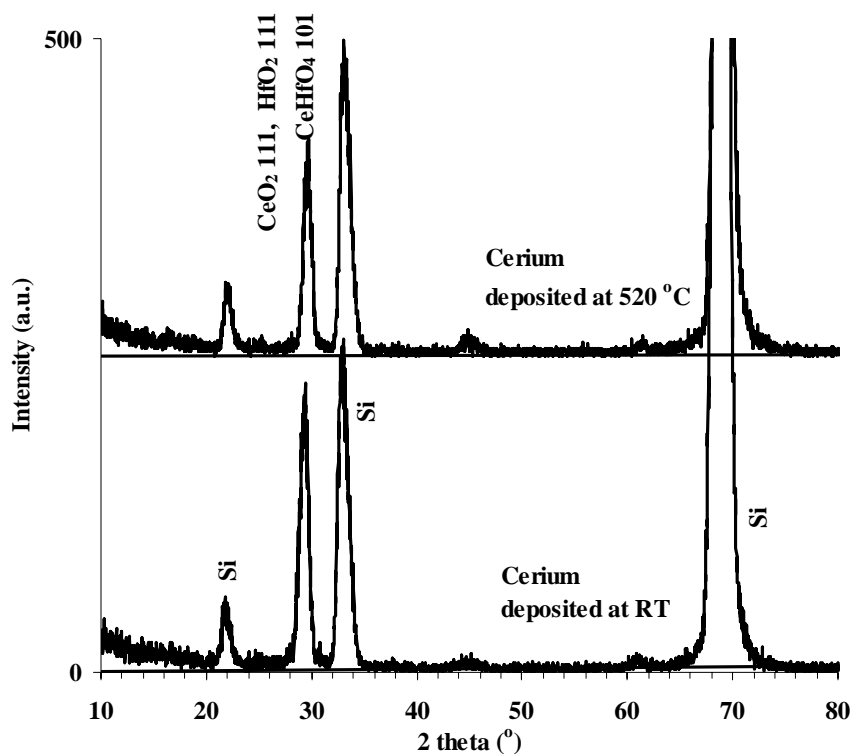
<sup>18</sup> Ion flux is monitored by the probes placed to the edge of evaporation pocket. Evaporation power is coupled to the ion flux for achieving a steady deposition rate.

<sup>19</sup> Evaporation pocket was a molybdenum crucible with a boron nitride (hexagonal) liner inside.

PLD parameters given in previous chapters, on cerium metal interlayer. Cerium interlayer deposition has been performed at room temperature for the first thickness series of the laminates, and at 520 °C for the second one<sup>20</sup>. An *in-situ* high oxygen pressure ( $p_{O_2}=100$  mbar) PDA with a cooling rate of a 5 °C/min is applied after all depositions to complete the oxidation of the layers.

#### 4.7.2. Results and Discussion

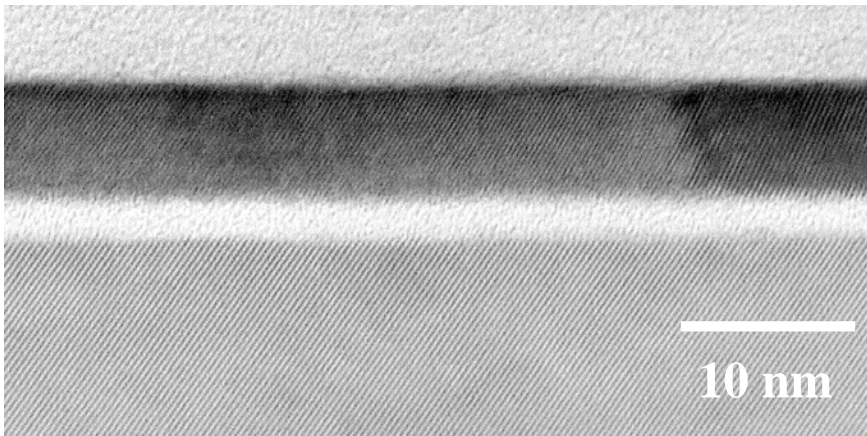
XRD analyses of the 16 nm laminates are presented in Figure 4.46. According to the figure, there are no significant differences between two cerium interlayer deposition temperatures. The layers shows a similar crystal structure with other laminates, deposited at same temperature without a cerium interlayer, as presented in earlier sections of this chapter.



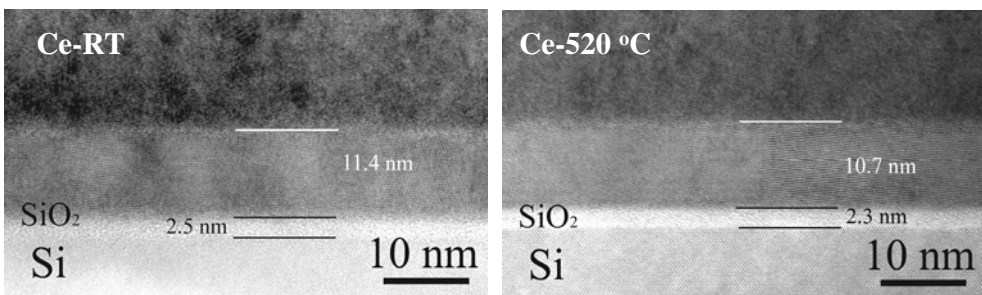
**Figure 4.46:** XRD patterns of the 16 nm CeO<sub>2</sub>-HfO<sub>2</sub> laminates deposited at 520 °C on cerium metal interlayer, which is deposited at room temperature (bottom) and 520 °C (top)

<sup>20</sup> Laminates with a cerium interlayer deposited at room temperature will be called as Ce-RT and the laminates with a cerium interlayer deposited at 520 °C will be called as Ce-520 °C, in the rest of the chapter. Note that, for both cerium deposition temperatures, the PLD is performed at 520 °C.

Since the 4 nm layers were not investigated by high resolution TEM, it is difficult to conclude about the thickness dependency of the layers, as already observed for the laminates without a cerium interlayer, which are presented in earlier sections. However, the cross sectional TEM image of the 8 nm Ce-RT layer (Figure 4.47) shows that the layer is ‘highly oriented’ (can be considered as epitaxial) and this may cause an increase in the dielectric constant. Cross sectional TEM images of Ce-RT and Ce-520 °C laminates with an estimated deposited thickness of 16 nm are shown in Figure 4.48. Images showed that the laminates are polycrystalline contrary to the 8 nm Ce-RT laminate, which is shown in Figure 4.47.



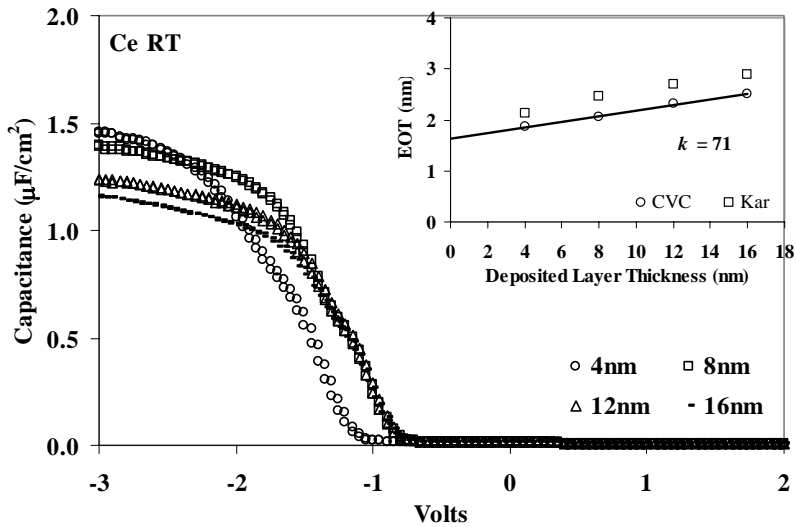
**Figure 4.47:** Cross sectional TEM image of the 8 nm Ce-RT laminate.



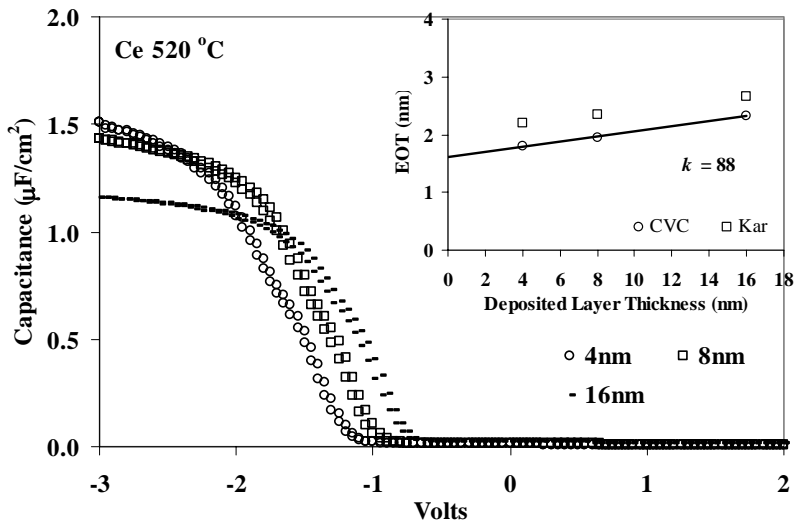
**Figure 4.48:** Cross sectional TEM images of Ce-RT and Ce-520 °C laminates with an estimated deposited thickness of 16 nm.

C-V analyses of the laminates, presented in Figure 4.49 and 4.50, are showed that the Ce-520 °C laminates have more hysteresis (80 mV) compared to the Ce-RT laminates (<50 mV). It’s also noted that C-V plots of the Ce-520 °C laminates are shifting to more positive voltages as the thickness increases, whereas the C-V plots of the Ce-RT laminates doesn’t show a shift for 8, 12 and 16 nm layers. The increased

hysteresis and a shift in  $C$ - $V$  plot to more positive voltages for the Ce-520 °C laminates indicates that the charge density in these layers is higher compared to the Ce-RT layers. EOT values extracted from the  $C$ - $V$  measurement are also presented in figures 4.49 and 4.50, and shows that the Ce-RT layers has  $k=71$  and Ce-520 °C layers has a  $k=88$ .



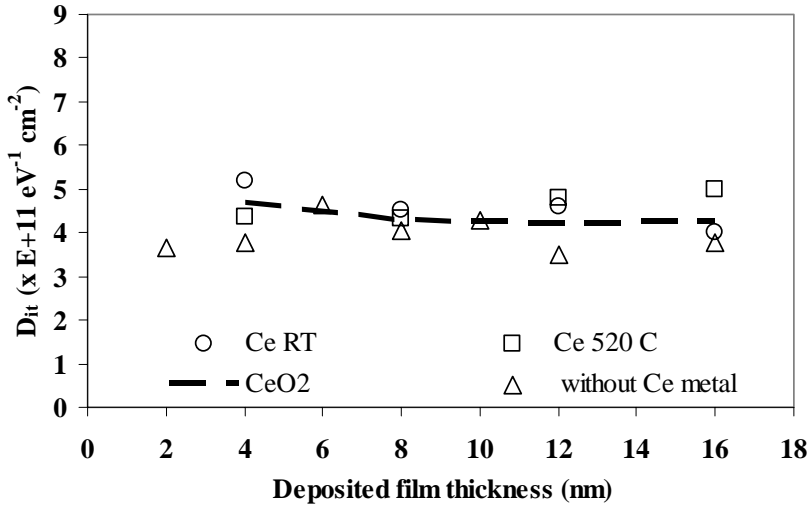
**Figure 4.49:**  $C$ - $V$  plots of the Ce-RT laminates with thicknesses from 4 to 16 nm. Inset shows the EOT values of the layers for different thicknesses, extracted by CVC simulation and the Kar method.



**Figure 4.50:**  $C$ - $V$  plots of the Ce-520 °C laminates with thicknesses from 4 to 16 nm. Inset shows the EOT values of the layers for different thicknesses, extracted by CVC simulation and the Kar method.



$D_{it}$  of the Ce-RT and Ce-520 °C laminates are compared to those without a cerium interlayer and CeO<sub>2</sub> reference layers deposited at 520 °C, in Figure 4.51. The figure shows that the  $D_{it}$  values of the layers are in the same level. This indicates that the presence of a cerium metal interlayer doesn't cause a significant change in the Si-CeO<sub>2</sub> interface.

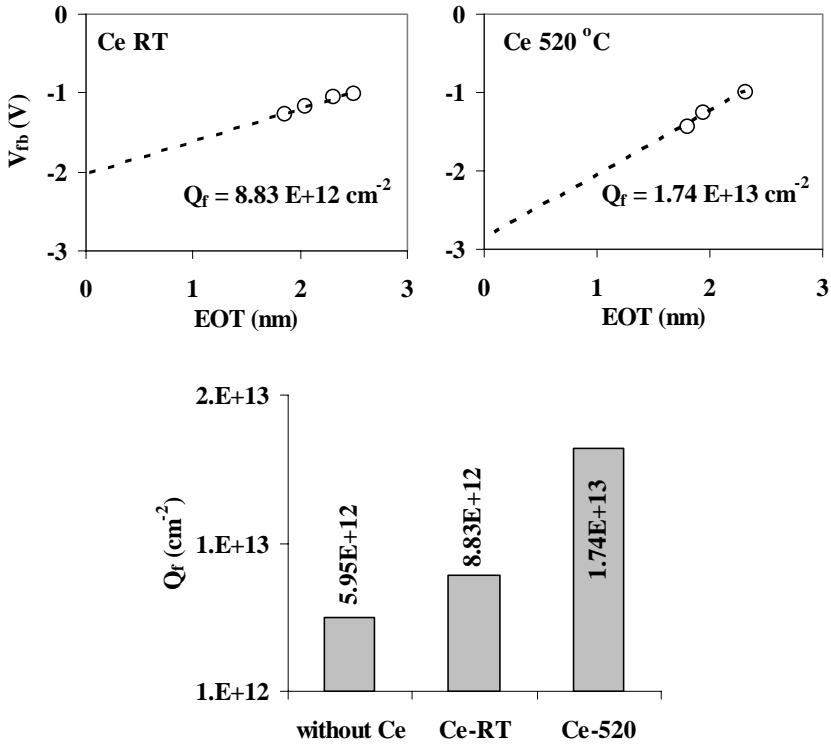


**Figure 4.51:**  $D_{it}$  values of the Ce-RT and Ce-520 °C laminates compared to those without cerium interlayer and to the CeO<sub>2</sub> reference layers deposited at same temperature.

$V_{fb}$  of the Ce-RT and Ce-520 °C laminates as a function of their EOT values are shown in Figure 4.52. Their  $Q_f$  values, extracted from the slope of the linear fit of  $V_{fb}$ -EOT plot, are also compared to the laminates without a cerium interlayer in the figure. It's found that the  $Q_f$  of the Ce-520 °C laminates are higher ( $Q_f=1.74 \times 10^{13} \text{ cm}^{-2}$ ) than Ce-RT laminates ( $Q_f=8.83 \times 10^{12} \text{ cm}^{-2}$ ), and both are higher than the laminates without a cerium metal interlayer. It indicates that incorporation of the cerium to the interface oxide is increasing the fixed charge density; in other terms, cerium enriched interface have more fixed charge than the one formed without a cerium metal interlayer. Work function differences of the Ce-RT ( $\phi_{ms}=2.03 \text{ eV}$ ) and Ce-520 °C ( $\phi_{ms}=2.87 \text{ eV}$ ) laminates are also found different, which is a result of different  $Q_f$  ( $Q_f > 10^{12} \text{ cm}^{-2}$  for both series) values of the layers. Another possible mechanism is silicide formation at the interface, which changes the band structure of the layers.

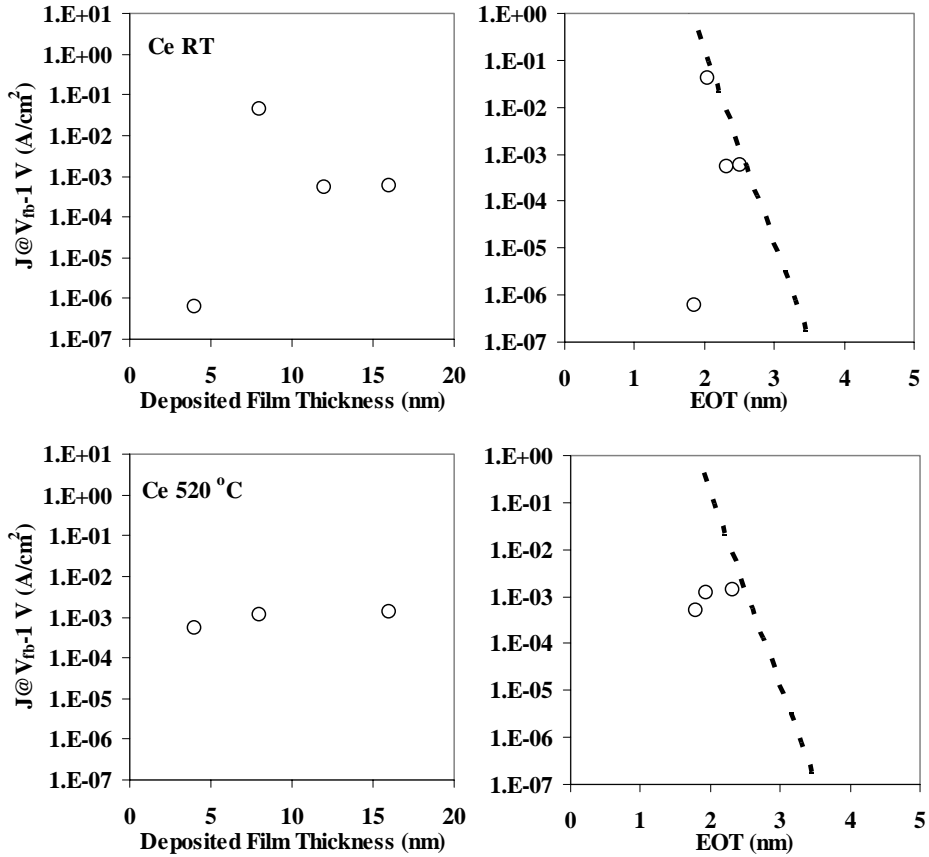
Leakage current densities of the layers are presented in Figure 4.53. It's been observed that the Ce-520 °C layers didn't show a leakage current reduction through increased physical thickness, as well as through EOT. Ce-RT layers, however, showed a different leakage current reduction trend than Ce-520 °C layers: The 4 nm Ce-RT laminate, which has an EOT of 1.87 nm, gave the best  $J$  ( $J_g @ V_{fb}-1 \text{ V}=3.1\text{E-}7 \text{ A/cm}^{-2}$ ). The 8 and 12 nm Ce-RT laminates shows a leakage current reduction with increased

physical thickness. This can be correlated to the presence of an amorphous phase in the 4 nm Ce-RT layer, whereas the 8 and 12 nm laminates have a highly oriented (or epitaxial) structures, which may suffer from the leakage through the grain boundaries.

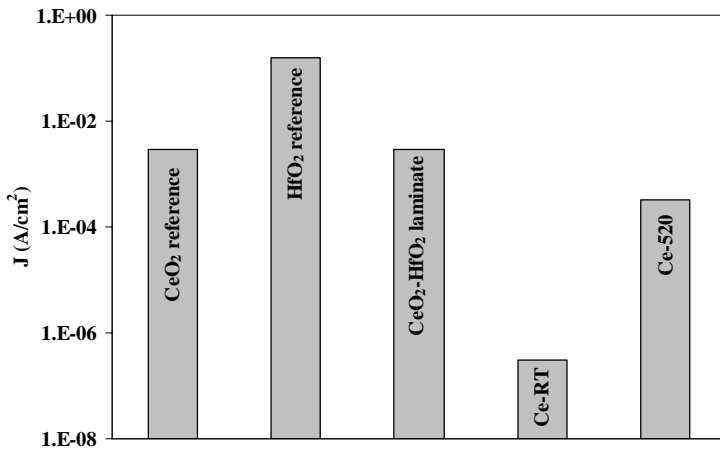


**Figure 4.52:**  $V_{fb}$ -EOT plots of Ce-RT (top left) and Ce-520 °C (top right) laminates. A comparison of the extracted  $Q_f$  values with the laminates without a cerium interlayer is also presented (bottom).

The leakage current densities of the 4 nm Ce-RT and Ce-520 °C layers are compared to the  $\text{CeO}_2$  and  $\text{HfO}_2$  reference layers, as well as to the  $\text{CeO}_2$ - $\text{HfO}_2$  laminated structure without a metallic cerium interlayer in Figure 4.54. Figure shows the remarkable low leakage current density for the 4 nm Ce-RT layer.



**Figure 4.53:** Leakage current densities of Ce-RT (top) and Ce-520 °C (bottom) laminates vs. deposited layer thickness (left) and vs. EOT (right). Dashed lines are SiO<sub>2</sub> reference data.



**Figure 4.54:** Leakage current densities of different layers with 4 nm thickness.

In conclusion, the 4 nm Ce-RT laminate, with an EOT=1.87 nm, showed the best leakage current density of  $J_g@V_{fb-1} V=3.1 \times 10^{-7} \text{ A/cm}^2$  compared to the other layers deposited at 520 °C. This is correlated to the presence of an amorphous phase in this layer. However, the laminates without a cerium metal interlayer, deposited at 520 °C were crystalline. This indicates that, for this deposition temperature, cerium metal interlayer deposited at RT increases the amorphous phase stability of the laminates. Additionally, the epitaxial (highly-oriented) laminate on an amorphous interface (Figure 4.47) indicates that the cerium metal interlayer can be used for manipulating the orientation behavior of the dielectric layers.

#### 4.8. Conclusions

It's found that the layer sequence in the laminated structure affects both, structural and electrical properties of the layers. The C-H-C-H layer sequence gave the best  $J$  compared to the other layer sequence, as well the CeO<sub>2</sub> and HfO<sub>2</sub> reference layers with the same thickness. This is correlated to the amorphous structure of the C-H-C-H laminate, whereas the other layers have a polycrystalline structure. This also shows that the laminates with that sequence have higher amorphous phase stability.

The lamination degree, in terms of the number of layers for a given thickness, is found to be affecting the properties of the layers. It's been observed that the  $C$ - $V$  hysteresis increases drastically with increasing individual layer thickness.

It is showed that the layers deposited in O<sub>2</sub> have better EOT- $J_g$  trade-off, and lower  $Q_f$  compared to those deposited in Ar+H<sub>2</sub>. However, the low  $k$  value ( $k=15$ ) of these layers was too low to fulfill the requirements for a high- $k$  dielectric. The layers deposited in Ar+H<sub>2</sub> has a  $k=30$ , in the case of the MOS devices with Au electrodes.

The effect of the deposition temperature on the laminates showed a transition from 420 to 620 °C deposition temperatures for 4 nm layers. EOT of the layers increases at this temperature range. This is correlated to a crystalline phase formation and oxidation of the interface with increasing temperature. The crystalline phase in the laminates is found to be tetragonal CeHfO<sub>4</sub> according to the XRD and TEM analyses. However, one should note that the crystallites also fit to CeO<sub>2</sub> and HfO<sub>2</sub>.

The thickness series of the laminates showed that the crystallinity of the layers increases with increasing thickness. This effect is more significant for lower deposition temperatures. This results in a wrong interpretation of the  $k$  value of the layers. EOT- $J_g$  of the layers also confirms a thickness dependent behavior of the layers; *i.e.* high leakage current in case of polycrystalline layers.

The effect of cooling rate in PDA showed that the crystallinity of the layers is decreasing by increasing cooling rate.  $Q_f$  of the layers didn't change significantly for

different cooling rates. This may indicate that the major effect of the cooling rates is on the crystallinity of the layers, as also confirmed by the  $J$  characteristics of the layers. Different oxidation times of the layers showed that the change in interface oxide properties occurs at the early stages of oxidation.

Improvement of the interface oxide by means of cerium metal interlayer deposition is investigated. It's been observed that the 8 nm Ce-RT layer have an epitaxial structure, where as the 16 nm laminates have a polycrystalline structure. The best  $J_g$  is achieved by the 4 nm Ce-RT layer. The  $J_g$  level of the layer is found to be similar to other amorphous 4 nm CeO<sub>2</sub>-HfO<sub>2</sub> laminates.

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# *Chapter 5*

## **Fabrication of MOSFETs with Nanolaminated CeO<sub>2</sub> - HfO<sub>2</sub> Gate Dielectrics**

### **Abstract**

Metal Oxide Semiconductor Field-effect Transistors (MOSFET) with CeO<sub>2</sub>-HfO<sub>2</sub> nanolaminated gate dielectric layers are demonstrated. It is found that the device performance is influenced by the interface formed between the high-*k* layer and the gate metal (Al). The effect of the gate metal and the process compatibility are discussed. The effect of TaN electrode processing on the interface characteristics of the laminates are presented as well.

## 5.1. Introduction

Integration of high- $k$  dielectrics into Metal Oxide Semiconductor Field-effect Transistors (MOSFETs) requires special attention to the gate electrode compatibility. Heavily doped polysilicon (poly-Si) gates have been the standard gate electrodes for silicon devices in CMOS technologies. Advantages like adjustable work function by doping, which permits engineering the threshold voltage ( $V_T$ ) and the process compatibility with SiO<sub>2</sub> gate dielectrics made poly-Si the favored electrode for MOSFET devices. However, high resistivity of poly-Si and limited carrier concentration causes a significant depletion layer. The depletion layer decreases the overall capacitance of the gate stack and limits the device performance. The dopant penetration problem also limits the use of poly-Si and defines the need for metal gates for scaled devices [1-3]. The interface between poly-Si and high- $k$  gate layers shares the same problem with silicon - high- $k$  interface in manner of thermodynamics of interface oxide forming reaction. Metal gates, however, offer more choices for meeting the thermodynamical requirements, as well as decreasing the thermal budget by removing the need for dopant activation step for poly-Si gates. The requirements for metal gates in MOSFET devices can be summarized as follows [4]:

- The work function needs to be compatible with silicon.
- High carrier density.
- Thermal/chemical stability with the high- $k$  layer.

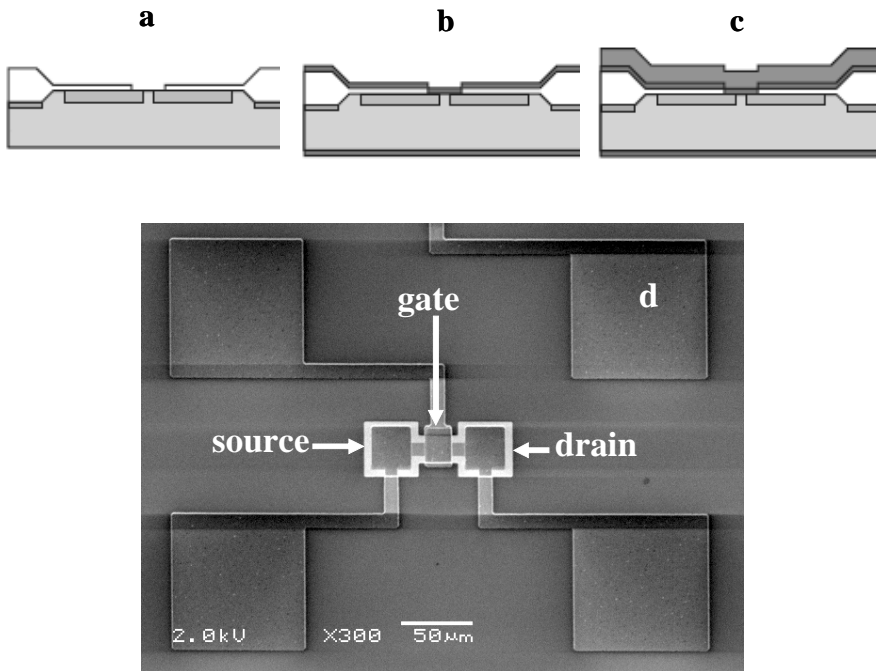
The performance of MOSFETs with high- $k$  dielectrics provides a good insight in understanding the issues of integrating metal gates with high- $k$  gate dielectrics. It is known from literature that MOSFETs with high- $k$  gate dielectrics show lower electron mobility as compared to devices with SiO<sub>2</sub> [5]. Coulomb scattering by interface traps and phonon scattering have been given as the major reasons for the lower electron mobility [6]. In this chapter, first results of MOSFET devices with CeO<sub>2</sub>-HfO<sub>2</sub> laminated dielectrics are demonstrated. The effect of the Al gate and the interface formed between the gate and the dielectric layer is discussed and the effect of capping layer on the Si – high- $k$  interface during electrode processing is presented.

## 5.2. Experimental

CeO<sub>2</sub>-HfO<sub>2</sub> laminates<sup>1</sup>, with thicknesses 4 and 7 nm, are deposited at 420 °C in 0.1 mbar Ar+H<sub>2</sub> (5%) with PLD on pre-patterned wafers (Figure 5.1) by using the deposition parameters described in Chapter 2. On top of the dielectric laminated layers, a 500 nm thick Al layer deposited by *in-situ* e-beam evaporation and *ex-situ* sputtering.

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<sup>1</sup> C-H-C-H sequence and an individual layer thickness of a 1 nm



**Figure 5.1:** Critical processing steps for gate dielectric deposition: (a) native oxide removal (b) gate oxide deposition (c) metallization. SEM image of the device, after all processing steps, is shown in d.

Aluminum layer of a 200 nm thickness is deposited *in-situ* at room temperature by e-beam evaporation<sup>2</sup>. The deposition rate is controlled by the ion flux at the evaporation source and a deposition rate of a 4 nm/min is achieved with a 50 nA ion flux. A secondary aluminum layer is deposited *ex-situ* by sputtering to give a total thickness of 500 nm. The wafers are then processed for making MOSFET devices and the critical part of the processing was performed for annealing of aluminum at 400 °C in  $N_2+H_2O$ <sup>3</sup> ambient for 30 minutes, as the final step of processing. Electrical characterization of NMOS devices with Al gate are performed with a HP 4145B analyzer.

TaN electrodes, discussed in the final section of this chapter, were deposited *ex-situ* by reactive sputtering and then electrode definition is performed by lithography and etching<sup>4</sup>. Etching of TaN electrodes is performed by plasma etching with  $CF_4$  and oxygen (10%).

<sup>2</sup> See Figure 4.45 for e-beam evaporator.

<sup>3</sup> Water vapor in contact with Al produces atomic hydrogen, which passivates the interface states as in forming gas anneal.

<sup>4</sup> See also Appendix 2 for electrode processing.

### 5.3. Device Operation.

The operation of the MOSFET is well-documented in literature [7 and 8]. For low source-drain voltage ( $V_{ds}$ ), the drain current  $I_d$  as function of the gate voltage  $V_g$  is given by:

$$I_d = \frac{W}{L} \mu C_{ox} (V_g - V_T) V_{ds}$$

where, W and L are the gate width and length,  $\mu$  is the channel carrier mobility,  $C_{ox}$  is the oxide capacitance and  $V_T$  is the threshold voltage.

The transconductance ( $g_m$ ) of a MOSFET is defined as [9]

$$g_m = \frac{\partial I_d}{\partial V_g}$$

K, the normalized transconductance, is excluded from gate dimensions and given as:

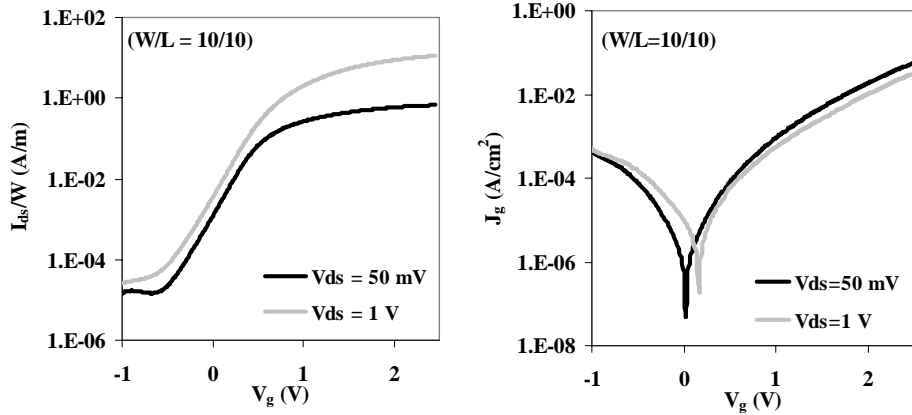
$$K = \frac{g_m}{V_{ds}} \frac{L}{W}$$

$K_0$  is the normalized transconductance given for very low  $V_{ds}$ , e.g. 50 mV, and is a measure of the channel efficiency

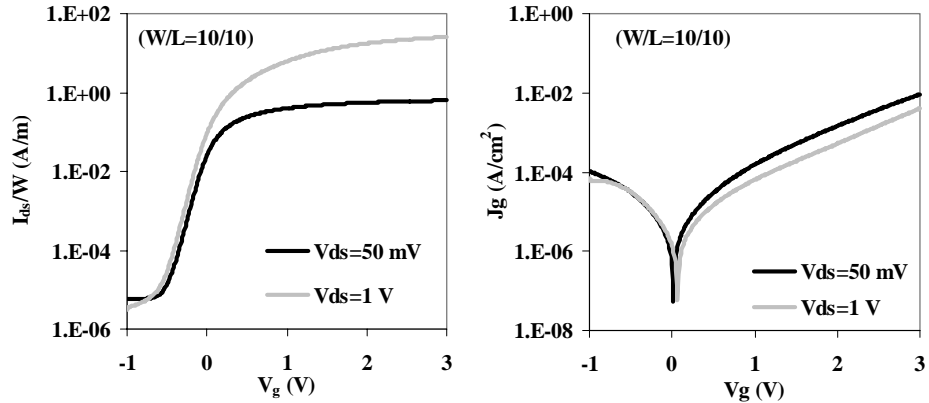
### 5.4. Results and Discussion

$I_d$  normalized by gate width as a function of  $V_g$  is shown in Figure 5.2 and Figure 5.3, for the NMOS with 4 and 8 nm gate dielectric thicknesses, respectively. For both devices the  $W/L=10/10$   $\mu\text{m}/\mu\text{m}$ . Corresponding gate leakage current densities ( $J_g$ ) are also presented in the figures. The threshold voltage ( $V_T$ ) of the device from the extrapolation of the linear section [10] of  $I_{ds}/W$  for  $V_{ds}=50$  mV, is found to be  $V_T=0.3$  V for 4 nm dielectric layer, whereas the one with 8 nm dielectric layer have a  $V_T= 0$  V.

$I_d$ - $V_{ds}$  of the same devices, with their normalized transconductances are shown in Figure 5.4 and 5.5 for the devices with dielectric layers of 4 and 8 nm, respectively. The maximum  $K_0$  of the devices is found  $K_0= 82$   $\mu\text{A}/\text{V}^2$  for 4 nm and  $K_0=95$   $\mu\text{A}/\text{V}^2$  for 8 nm laminates.



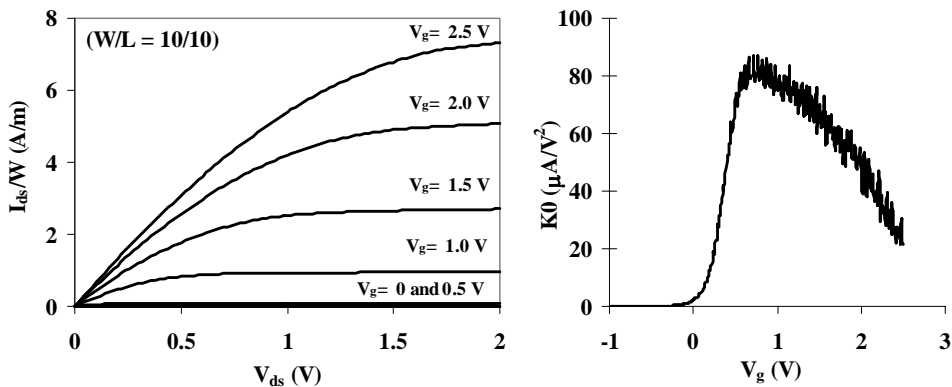
**Figure 5.2:**  $I_{ds}/W$  as a function of gate voltage (left) and corresponding leakage current densities (right) of NMOS device with a 4 nm laminated gate dielectric.



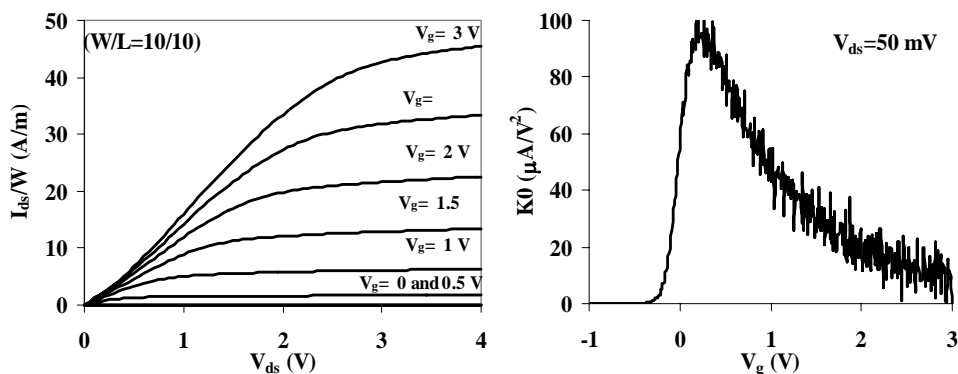
**Figure 5.3:**  $I_{ds}/W$  as a function of gate voltage (left) and corresponding leakage current densities (right) of NMOS device with 8 nm laminated gate dielectric.

The drive current at  $V_{ds} = 1$  V and  $V_g = V_{ds}$  was found to be  $2.1 \mu\text{A}/\mu\text{m}$  and  $6.2 \mu\text{A}/\mu\text{m}$  for the devices with 4 and 8 nm dielectric layers, respectively.  $J_g$  at  $V_{ds}=1$  V and  $V_g=V_{ds}$  of the devices with 4 and 8 nm dielectric layers were  $5.88 \times 10^{-4}$  A/cm<sup>2</sup> and  $6.39 \times 10^{-5}$  A/cm<sup>2</sup>, respectively.

The devices were characterized using TEM analysis. The cross sectional TEM image presented in Figure 5.6 shows the channel region of NMOS device. Two observations were made. First, it was found that the channel layer contained defects. These defects are possibly implant damage. Secondly, an amorphous layer was detected between the Al gate electrode and the dielectric layer. The interface between *in-situ* and *ex-situ* deposited Al layers is also visible in the image. According to the figure, the aluminum layer is largely polycrystalline and a distinct interface is formed between the *in-situ* and *ex-situ* deposited aluminum.

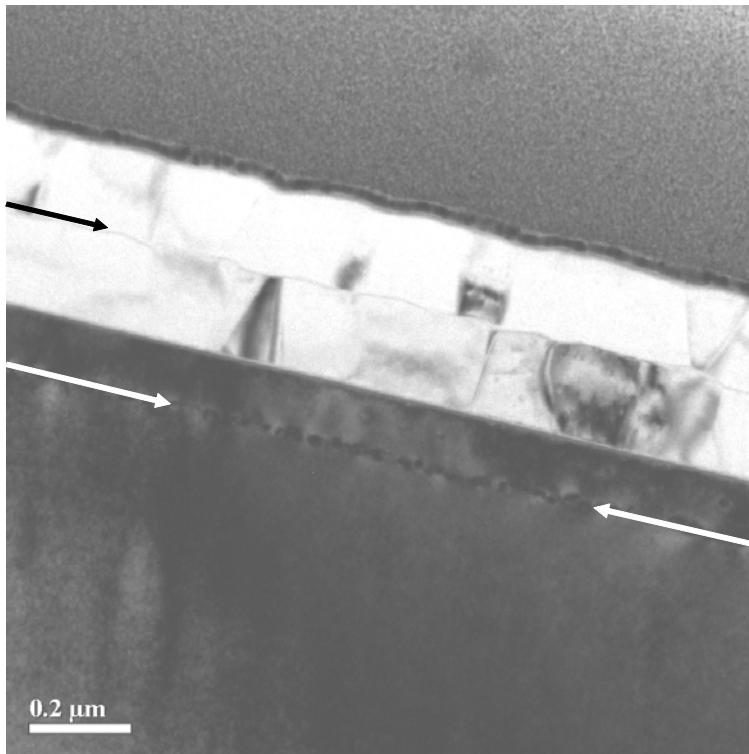


**Figure 5.4:**  $I_{ds}/W$  as a function of  $V_{ds}$  (left) and  $K_0$  as a function of  $V_g$  (right) of the NMOS device with 4 nm laminated dielectric.

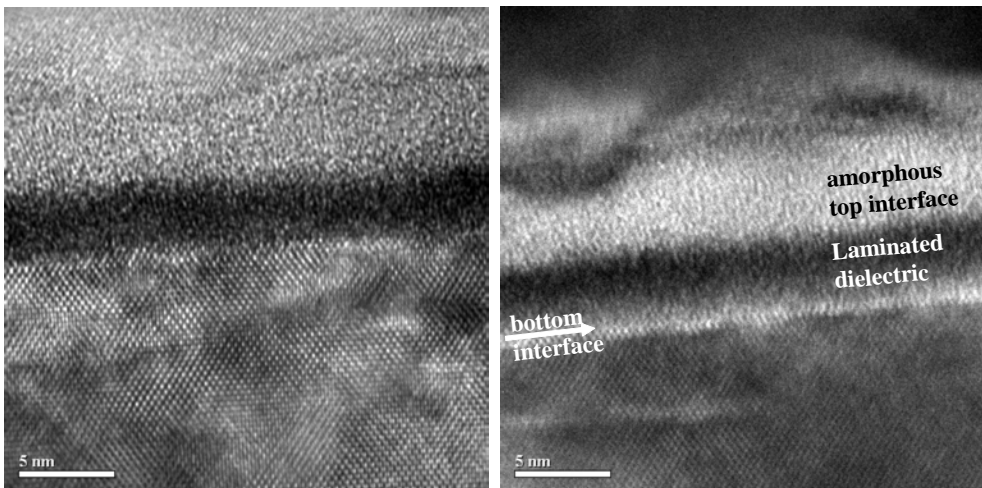


**Figure 5.5:**  $I_{ds}/W$  as a function of  $V_{ds}$  (left) and  $K_0$  as a function of  $V_g$  (right) of the MOSFET with 8 nm laminate dielectric.

High-resolution TEM (HR-TEM) and Energy-filtered TEM (EF-TEM) images showing the dielectric layer and its interfaces in details are presented in Figure 5.7. The EF-TEM image was filtered for  $24 \pm 2.5$  eV, the typical plasmon loss energy of  $\text{Al}_2\text{O}_3$ . Areas containing  $\text{Al}_2\text{O}_3$  appear bright. It is clearly visible that an amorphous layer (top interface) is present between the laminate and the Al electrode. An additional image with a High Angle Annular Dark Field Detector (HAADF) which gives the Z-contrast image (Figure 5.8) showed that the amorphous top interface layer did not contain the elements in the high- $k$  dielectric. Finally, Electron Energy Loss Spectrometry (EELS) analysis was used to investigate the top interface. It was found that the layer contained both oxygen (35%) and aluminum (65%). From this, it was concluded that the amorphous layer is mainly  $\text{Al}_2\text{O}_3$ .

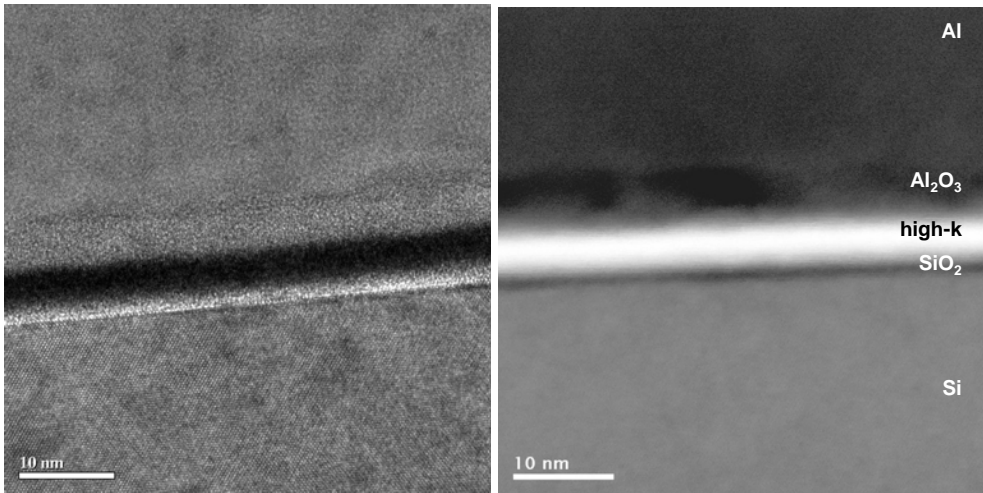


**Figure 5.6:** Cross sectional TEM image of the NMOS device. White arrows indicate the defects in the channel region of the device. Black arrow shows interface between the *in-situ* and *ex-situ* deposited Al layers. Scale bar is 200 nm.

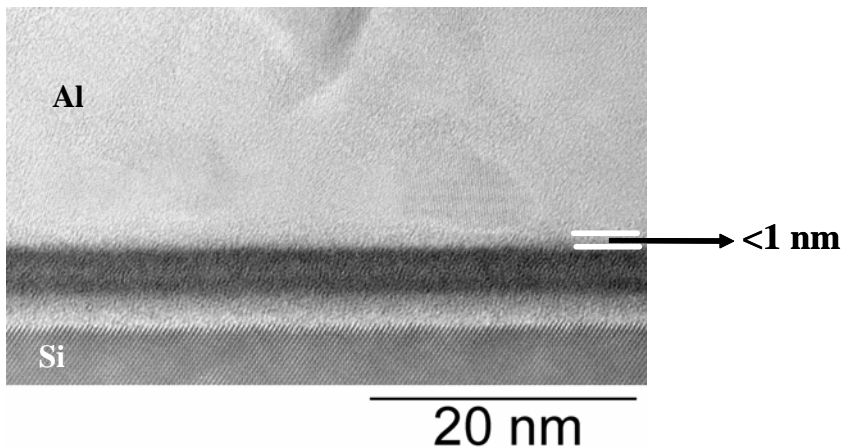


**Figure 5.7:** Cross sectional TEM (left) and EFTEM (right) images of the NMOS device showing the presence of the amorphous top interface. Note that, the bottom interface oxide thickness is in level of a monolayer. Scale bar of the images is 5 nm.

It's also noted that the bottom interface thickness was significantly thinner than that observed for similar laminates deposited at the comparable conditions and presented in the previous chapter. This might be caused by the reduction of the bottom interface oxide for forming a top interface during thermal treatment of the gate stack.



**Figure 5.8:** Cross sectional TEM (left) and the corresponding Z-contrast image (by HAADF) of the MOS structure showing that the top interface layer doesn't contain any of the elements present in high- $k$  dielectric.



**Figure 5.9:** Cross sectional TEM image of the laminated dielectric with an in-situ grown polycrystalline aluminum layer on top, didn't expose to any thermal treatment.



In order to understand when this top interface layer is formed, an additional experiment was performed using the identical dielectric deposition conditions but did not pass through the MOSFET processing steps, *i.e.* no thermal treatments applied after *in-situ* aluminum layer deposition. Cross sectional TEM image of the laminate with an *in-situ* deposited aluminum layer on top is shown in Figure 5.9. It's observed that the amorphous top interface thickness is less than 1 nm and Si - high-*k* interface is still present, compared to the monolayer interface thickness in the layer with a top interface. The composition of the top amorphous oxide is not analyzed; therefore it's not known that this interface is formed by Al<sub>2</sub>O<sub>3</sub> or amorphous aluminum. It's also noted that the laminated structure is still visible in the layer, contrary to the layer exposed to thermal treatment during MOSFET processing.

The difference between the interface oxide thicknesses of the laminates with aluminum capping layer before and after thermal treatment, shows that the formation of an upper interface affects the thickness of the Si – high-*k* interface. This indicates the reduction of the bottom interface oxide for forming the top interface during thermal processes. A similar process has been shown by Kim *et al.* [11], in case of Ti and Al layers deposited on HfO<sub>2</sub> and ZrO<sub>2</sub>. They also observed that the Si - high-*k* interface oxide reduces by formation of a top interface.

#### *The Effect of TaN Capping Layers on Si-High-k Interface during Processing*

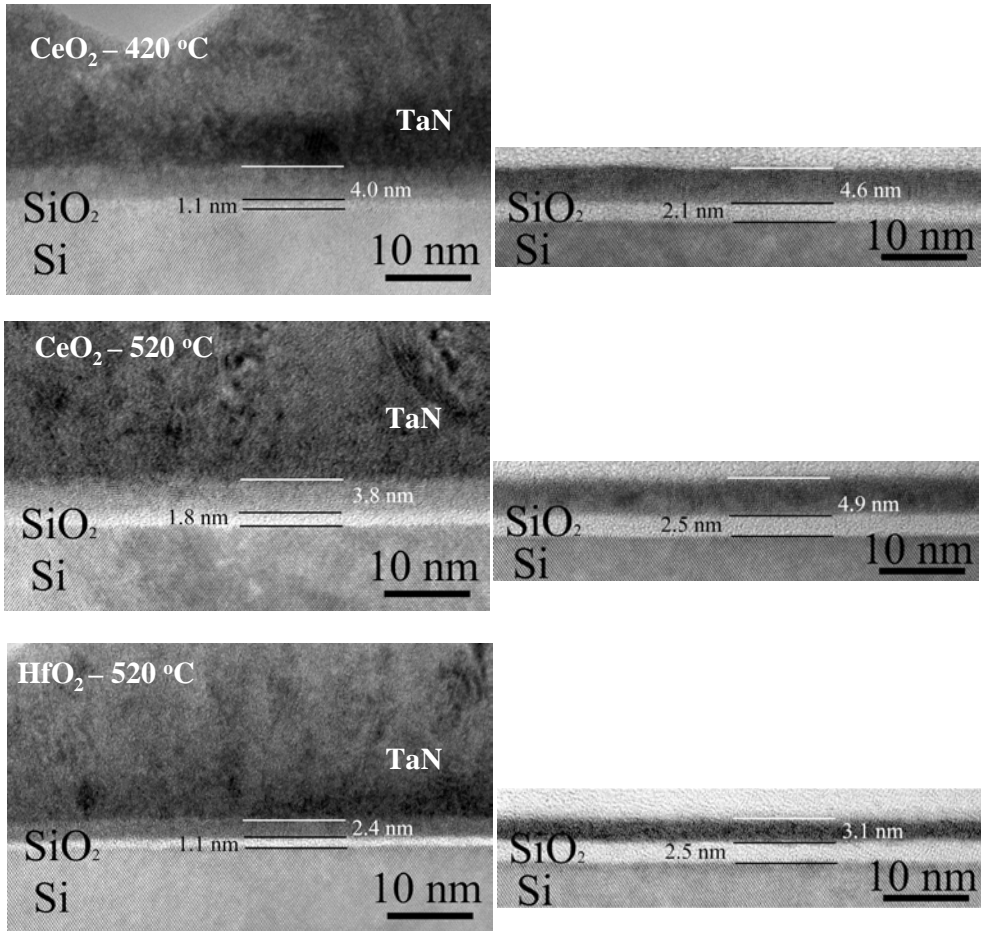
The effect of the TaN capping layers on the Si–high-*k* interface thickness during plasma etching in an oxidizing ambient<sup>5</sup> is observed in the TEM analysis of the layers (both, single oxides of CeO<sub>2</sub> and HfO<sub>2</sub> and their laminates).

As shown in Figure 5.10, in 4 nm layers, the areas with a TaN capping layers shows thinner interface than those without a capping layer on top. However, as presented in Figure 5.11, the 16 nm layers didn't show a big difference in interface oxide thicknesses for the areas with and without the capping layer. Different increases in interface oxide thicknesses for the thin and thicker layers indicates that an oxygen diffusion driven process is dominant rather than thermal effects during processing. This result indicates a potential problem in device processing as formation of 'bird beak'<sup>6</sup>

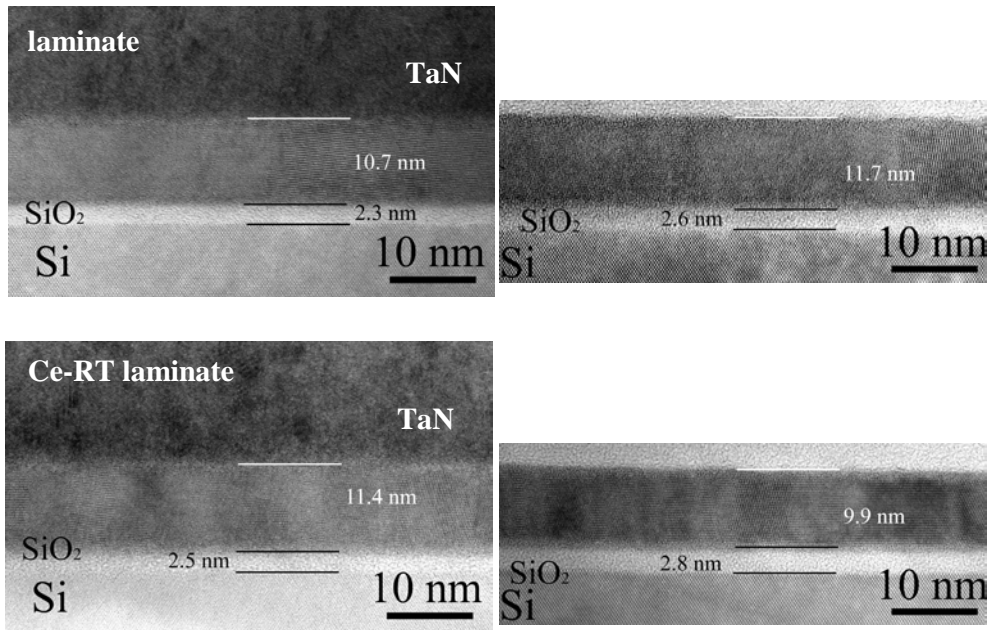
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<sup>5</sup> The most probable processing step for increasing the interface oxide is plasma etching of the electrodes. However, one should note that the wafers exposed to air for approximately one month before TEM analysis. Thus, further oxidation may also occur during wafer storage.

<sup>6</sup> Bird beak term is used to describe the interface oxide formation starts under the spacers and moves towards to the gate are, in a similar shape of a bird beak.



**Figure 5.10:** Cross sectional TEM images of the CeO<sub>2</sub> and HfO<sub>2</sub> reference layers of 4 nm deposited layer thickness, with (left) and without (right) TaN capping layer, showing the difference in the interface oxide thickness.



**Figure 5.11:** Cross sectional TEM images of different  $CeO_2$ - $HfO_2$  laminates with (left) and without (right) TaN capping layer. Estimated deposited layer thickness was 16 nm for both layers.

## 5.5. Conclusions

MOSFETs with laminated  $CeO_2$ - $HfO_2$  gate dielectric layers were demonstrated. The low  $K_0$  of the devices was correlated to defects in the channel region and to the formation of an amorphous  $Al_2O_3$  interface layer between the Al gate electrode and the  $CeO_2$ - $HfO_2$  laminate. This layer decreases the gate capacitance and hence reduces the drive current  $I_{ds}$ . It is found that the Si-high- $k$  interface oxide reduces by Al metal gate to form a top interface, between gate and dielectric layer. This process by formation of a top interface may lead to a potential approach for modification of Si – high- $k$  interface. However, one should take into account the thickness of the upper interface oxide and its contribution to the EOT of the dielectric with an increased total physical thickness.

Effect of capping layer on the interface oxide thickness during processing in an oxidizing ambient is presented. It is found that the TaN electrode layer prevents oxygen diffusion towards interface, as the areas without electrode layer showed an increase in the interface oxide thickness. This is indicated as a potential problem as ‘bird beak’ formation.

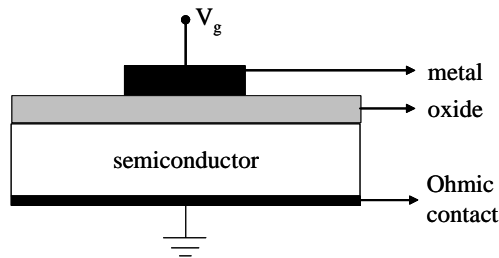
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# Appendix 1

## Electrical Characterization of MOS Devices with High- $k$ Dielectric Layers

The electrical characterization of high- $k$  gate dielectrics is an extremely important part of gate dielectric research. High- $k$  dielectrics typically have higher interface state density ( $D_{it}$ ), higher oxide charges and lower conduction band offset on silicon than  $\text{SiO}_2$  [1 and 2]. Therefore, some aspects of electrical characterization of Metal Oxide Semiconductor (MOS) devices with high- $k$  dielectric layers (Figure 1) differ from the ones with  $\text{SiO}_2$  layers and require a specific attention.



**Figure 1:** Schematic drawing of a MOS device.

Some crucial gate dielectric properties which can be extracted from  $C$ - $V$  measurements are:

- Equivalent oxide thickness (EOT).
- Interface and Oxide charges
- Flatband voltage ( $V_{fb}$ ).
- Work function difference of gate and silicon substrate ( $\phi_{ms}$ ).

In this work, p-type<sup>1</sup> MOS structures are used for electrical characterization of gate dielectrics. Data collection from MOS devices by  $C$ - $V$  and  $I$ - $V$  measurements, processing of raw data and data extraction from measurements are presented.

### 1. Measurement Setup and Data Acquisition

A Karl Suss PM-8 manual probe station equipped with HP4275A Analyzer and HP4140B pA-Meter is used for  $C$ - $V$  and  $I$ - $V$  measurements of MOS devices. The probe station and analyzers were connected to a computer system with MDC™ Measurement software<sup>2</sup>, which can control the voltage sweep range and rate and collects data.

<sup>1</sup> Boron doped ( $N_a=2 \cdot 10^{15} \text{ cm}^{-3}$ ) Si (001) wafers are used in this study.

<sup>2</sup> See the web site of the company for details: [www.mdc4cv.com](http://www.mdc4cv.com)

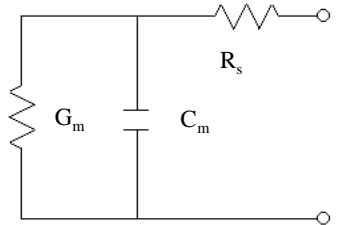
All measurements are performed at room temperature and a voltage sweep rate of a 50 mV/s is used<sup>3</sup>. Measurements are done for different electrode areas to prevent the errors that may result from area scaling. It should be noted that even the smallest electrode area used in this study (100 x 100 μm<sup>2</sup>) is large enough compared to the dielectric layer thicknesses (16 nm maximum), to neglect the effect of electric field broadening at electrode edges.

C-V measurements were performed at  $f=10$  kHz,  $f=100$  kHz and  $f=1$  MHz sweeping from inversion to accumulation and back.

I-V measurements are performed at two steps<sup>4</sup>: First, from zero bias to positive and then from zero bias to negative voltages till breakdown.

## 2. Series Resistance Correction of Capacitance – Voltage Measurements

Series resistance ( $R_s$ ) originates from probe-to-electrode contact, backside contact of substrate to chuck and resistance of bulk silicon. Extraction of the oxide capacitance from the measured capacitance ( $C_m$ ) and the conductance ( $G_m$ ) starts with series resistance correction and therefore requires re-modeling the equivalent circuit from basic two element parallel mode by a model which includes the series resistance. The actual circuit is presented in Figure 2, by adding the series resistance component to the parallel circuit in the measurements.



**Figure 2:** Actual circuit for capacitance measurements includes the series resistance.

The method developed for series resistance correction of leaky gate dielectrics have been proposed by Yang and Hu [3]. This method, known as dual frequency correction (DFCR), is used for eliminating the effect of measurement frequency and results in frequency and series resistance independent capacitance. The impedance of three element circuit in Figure 3.2 is:

$$Z = R_s + \frac{R_p (1 - j\omega C R_p)}{1 + \omega^2 C^2 R_p^2} \quad (1)$$

<sup>3</sup> Sweep rate affects the charge trapping behavior of MOS device, therefore is kept constant for all measurements for comparison purposes.

<sup>4</sup> Details of I-V measurement are given in following sections of this chapter.

where  $R_p$  is the parallel resistance that is inverse of  $G_p$  ( $R_p = 1/G_p$ ). The impedance of the parallel circuit in Figure 2 is:

$$Z = \frac{D - j}{\omega C_m (1 + D^2)} \quad (2)$$

where  $D$  is the dissipation factor, which is given as:

$$D = \frac{1}{\omega R_m C_m} \quad (3)$$

$R_m$  and  $C_m$  correspond to the measured values.

By equating the imaginary parts of the measured impedance of parallel circuit and the true impedance of actual circuit, the following relation is obtained:

$$\frac{1 + \omega^2 C^2 R_p^2}{C R_p^2} = \omega^2 C_m (1 + D^2) \quad (4)$$

Solving the Eq. (4) for the real capacitance ( $C$ ):

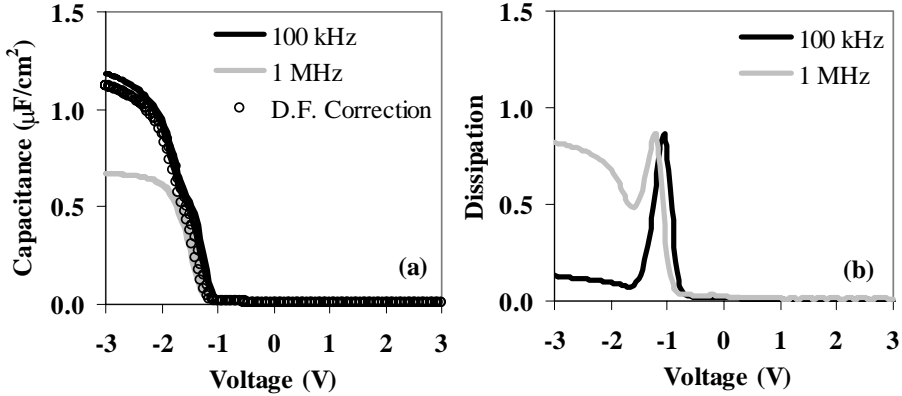
$$C = \frac{f_1^2 C_{m1} (1 + D_1^2) - f_2^2 C_{m2} (1 + D_2^2)}{f_1^2 - f_2^2} \quad (5)$$

where,  $C_{m1}$  and  $D_1$  refer to the first measurement frequency ( $f_1$ ),  $C_{m2}$  and  $D_2$  to the second measurement frequency ( $f_2$ ).

Nara *et al.* proposed a guideline for applicability limits of dual frequency correction in order to keep the error of oxide thickness determination below 4% [4]. According to them, dissipation should remain below 1.1 for fulfilling the ITRS measurement error requirements. In this work  $f=100$  kHz and  $f=1$  MHz were used for dual frequency correction<sup>5</sup>. This conditions satisfy the dissipation condition for most of the MOS devices investigated.

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<sup>5</sup> 100 kHz is chosen as the lower limit because frequencies lower than 100 kHz are extremely sensitive to interface traps and oxide charges.



**Figure 3:** (a) measured capacitance ( $f_1=100$  kHz and  $f_2=1$  MHz) and dual frequency corrected capacitance, according to Eq. (5) (b) Dissipation factor ( $D$ ) as a function of the applied voltage.

The measured  $C$ - $V$  curves of 4 nm  $\text{CeO}_2$ - $\text{HfO}_2$  laminated layer and the dual frequency corrected capacitance are shown in Figure 3.a. The corresponding dissipation factor is presented in Figure 3.b. Dissipation at accumulation (voltage  $\leq -2$  V) remains below the suggested limit of 1.1.

### 3. Determination of Equivalent Oxide Thickness

The EOT of a high- $k$  gate dielectric is defined as the thickness of  $\text{SiO}_2$  ( $k=3.9$ ), which gives the same capacitance with the high- $k$  dielectric with a higher dielectric constant [5-7] and given as:

$$EOT = t_{high-k} \frac{\kappa_{\text{SiO}_2}}{\kappa_{high-k}} \quad (6)$$

where,  $t_{high-k}$  is the physical thickness of high- $k$  dielectric and  $\kappa_{high-k}$  is the relative dielectric constant of high- $k$  dielectric. However, it has to be noted that the EOT of the gate stack extracted from the  $C$ - $V$  data is the sum of high- $k$  layer and the interface:

$$EOT = EOT_{IL} + EOT_{high-k} \quad (7)$$

where  $EOT_{IL}$  is the EOT of the interface layer.

In this work, two methods are chosen for EOT determination: One is based on quantum mechanical simulation including the gate depletion effect, a computer program called CVC [8], which is used by a majority of researchers for extracting the oxide parameters. This method assumes the contribution of interface states and bulk oxide charges on accumulation capacitance can be neglected for high frequency measurements. It is also assumed that an infinite potential barrier is present at the silicon-dielectric interface.



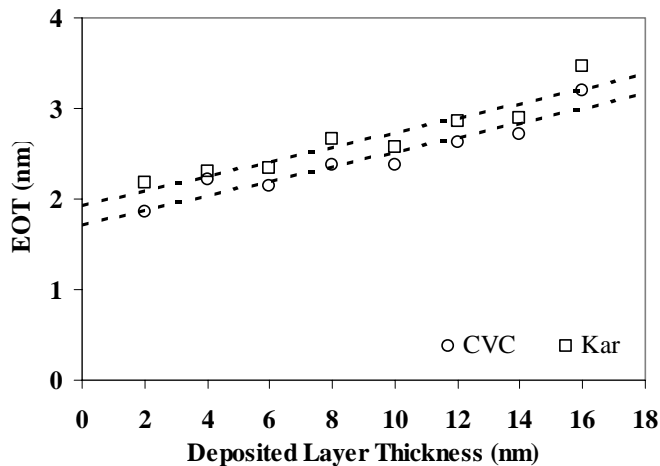
The second method is the oxide capacitance determination by a model developed by Kar, which assumes that contribution of both the space charge and the interface states are exponential functions of the surface potential in accumulation regime of C-V plot. [9].

The CVC simulation program is reconstructing the C-V plot based on the experimental data by using the following parameters:

- electrode area
- substrate type and doping level
- substrate temperature
- polysilicon depletion and polysilicon doping level

The method proposed by Kar uses a linear fit of a plot of  $C^{-1}$  versus  $|dC^{-2}/dV|^{-2}$  in strong accumulation. This intercepts with the x-axis and yields in reciprocal capacitance ( $1/C$ ), where  $C$  is the oxide capacitance that is used for the EOT calculations.

Using these two methods in parallel on the same experimental data, provides a double check of the results and therefore minimizes the risk of data extraction errors. Figure 4 shows the EOT values found by two methods for a thickness series of 520 °C deposited CeO<sub>2</sub>-HfO<sub>2</sub> laminated dielectrics. The difference in between the results of two different EOT extraction methods (varies from 4% to 20%) yields in different EOT intersection of linear fits of plots, which is used to determine the EOT<sub>IL</sub>.



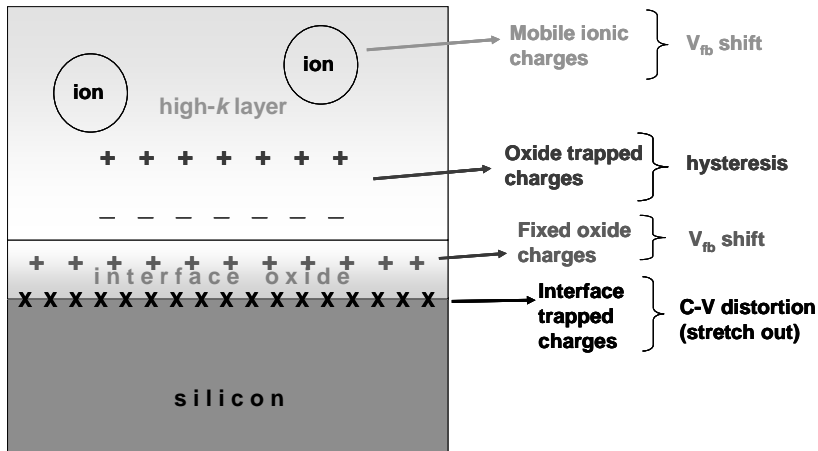
**Figure 4:** EOT versus deposited layer thickness plot based on two different EOT extraction methods. CVC simulation (open circle) gives lower EOT value than linear fit in strong accumulation method (square).

One should note that the error level in EOT extraction for each method depends on the errors in the C-V measurement (e.g. electrode area scaling, measurement

temperature and calibration of measurement setup), series resistance correction (a dissipation factor below 1.1) and the method itself. Applying a proper simulation in CVC and double checking the results with the Kar method, keeps the error margin of EOT determination in level of 5-7%, for proper  $C-V$  measurement.

#### 4. Determination of Interface and Oxide Charges

Oxide charges, shown in Figure 5, are localized at different positions in the MOS structure and have different effects on the  $C-V$  behavior of the device. Their characterization is an important step in understanding the characteristics of a silicon-oxide system. Interface trapped charges ( $Q_{it}$ ), fixed oxide charges ( $Q_f$ ), oxide trapped charges ( $Q_{ot}$ ) and mobile oxide charges ( $Q_m$ ) are the four types of charges that exist in a MOS structure. In this part, methods for charge determination used are described.



**Figure 5:** Schematic illustration of interface and oxide charge locations and their effect on  $C-V$  characteristics.

##### 4.1. Determination of Interface State Density

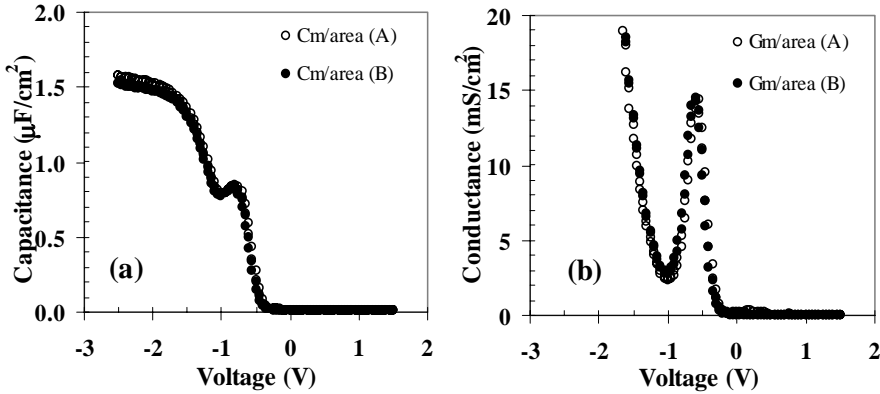
Interfaces trapped charges ( $Q_{it}$ ), defined by their densities per area in terms of density of interface states ( $D_{it}$ ), and are pointed out as one of the major problems of implementation of high- $k$  dielectrics CMOS applications. Interface trapped charges are originated by structural defects, defects induced by oxidation, impurities at interface and radiation effects (or any other effect causes bond breaking at silicon interface) [10 and 11].

Carter *et al.* presented an efficient technique based on conductance measurements of a  $\text{SiO}_2 - \text{HfO}_2$  gate dielectric system [12]. The technique uses the peak conductance data for  $f=10$  kHz. According to the described method, density of interface states ( $D_{it}$ ) is written as:

$$D_{it} = \frac{0.4(G_p / \omega)}{qA} \quad (8)$$

where  $G_p$  is the peak conductance in the parallel  $C$ - $V$  measurement configuration,  $A$  is electrode area and  $q$  is the elementary charge.

Measurements from different electrode areas are normalized by the electrode area and then plotted versus gate voltage to find the peak conductance ( $G_p$ ). Figure 6.a and 6.b shows the area normalized  $C$ - $V$  and  $G$ - $V$  data of the MOS device with 2 nm  $\text{CeO}_2$ - $\text{HfO}_2$  laminate, measured on two different electrode areas at 10 kHz.



**Figure 6:** (a)  $C$ - $V$  data ( $f=10$  kHz) of 2 nm thickness laminated dielectric, deposited at  $420^\circ\text{C}$ . (b)  $G$ - $V$  plot of the same device showing the  $G_p$  that is used for  $D_{it}$  calculation by Eq. (8).  $C_m$  and  $G_p$  are normalized by two different electrode areas (electrode A:  $100 \times 100 \mu\text{m}^2$  and electrode B:  $200 \times 200 \mu\text{m}^2$ ).

## 4.2. Determination of Fixed Oxide Charges

Oxide fixed charges ( $Q_f$ ), located at the silicon – high- $k$  interface, are determined by using the definition of flatband voltage:

$$V_{fb} = \phi_{ms} \pm \frac{Q_f}{C} \quad (9)$$

where  $\Phi_{ms}$  is work function difference between silicon substrate and metal gate electrode [13 and 14]. Eq. (9) can also be written as follows:

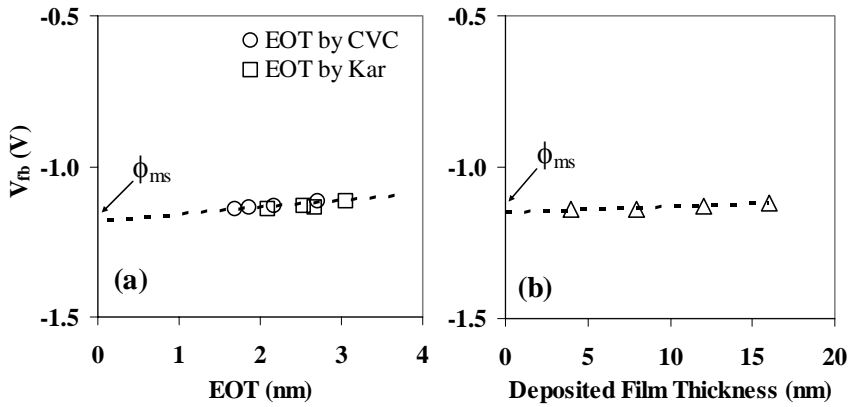
$$V_{fb} = \phi_{ms} \pm \frac{Q_f}{\epsilon_o \epsilon_{\text{SiO}_2}} EOT \quad (10)$$

where  $\epsilon_o$  is the permittivity of vacuum and  $\epsilon_{\text{SiO}_2}$  the permittivity of  $\text{SiO}_2$ . For extracting fixed oxide charge from flatband voltages of various layer thicknesses, one should plot

flatband voltage versus EOT<sup>6</sup> and the linear fit of such plot would yield on effective work function difference and the slope of linear fit will give the fixed oxide charge density of dielectric material.

$V_{fb}$  is plotted versus EOT and the deposited layer thickness in Figure 7 (Data used in this plot belongs to CeO<sub>2</sub> layers deposited at 520 °C). Note the difference between EOT and the deposited layer thickness plots. In order to minimize the errors, using EOT instead of deposited layer thickness gives more accurate results because it includes the contribution of both high- $k$  and interface layers on capacitance and doesn't affected by physical thickness measurement errors. As can be seen in the, intersections of linear fits for EOT (Figure 7.a) and for deposited layer thickness (Figure 7.b) are different. This leads to two different  $\phi_{ms}$  for the same device, which is not realistic.

Differences of EOT determination methods, as described earlier in this chapter, can also cause fixed oxide charge calculation and  $\phi_{ms}$  determination errors. Therefore one should always indicate the method for EOT extraction when using this method for fixed oxide charge calculation. It also has to be noted that errors in flatband voltage determination may increase the error of fixed oxide charge calculations.



**Figure 7:** Flatband voltage plotted versus EOT (a) by two different EOT extraction methods and versus deposited layer thickness (b), for the CeO<sub>2</sub> layers deposited at 520 °C. Dashed lines are the linear fits of plots, intersects at the work function difference.

### 4.3. Determination of Oxide Trapped Charges

Oxide trapped charges ( $Q_{ot}$ ) are distributed throughout the oxide.  $Q_{ot}$  is defined by the shift of flatband voltage, which can be written as follows [15]:

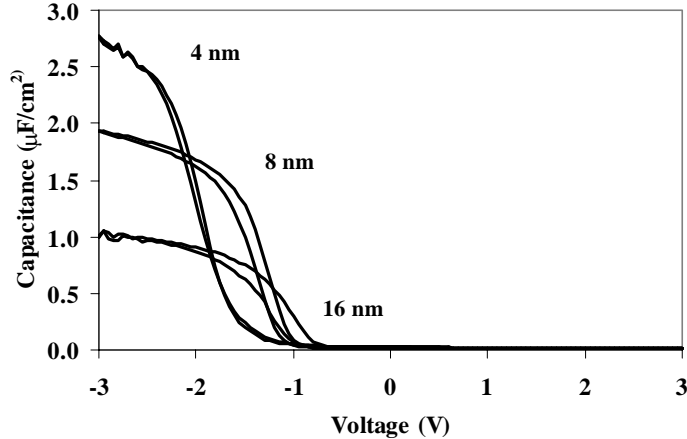
<sup>6</sup> Physical layer thickness can also be used in equation 3.11 by using the actual dielectric constant of the high- $k$  layer instead of the permittivity of SiO<sub>2</sub>.

$$\Delta V_{fb} = V_{fb}(Q_{ot}) - V_{fb}(Q_{ot} = 0) = -\gamma \frac{Q_{ot}}{C} \quad (11)$$

where  $\gamma$  is showing the charge distribution factor. Assuming that the  $V_{fb}$  shift is only caused by  $Q_{ot}$  and  $\gamma=1$ ,  $\Delta V_{fb}$  is then:

$$\Delta V_{fb} = -\frac{Q_{ot}}{C} = -\frac{Q_{ot}}{3.9\epsilon_0 A} EOT \quad (12)$$

According to (12),  $Q_{ot}$  can be determined by the slope of the plot of  $\Delta V_{fb}$  versus EOT. The change in C-V hysteresis ( $\Delta V_{fb}$ ) is used to compare the results from the measurements of different layer thicknesses. In Figure 8, an example of C-V showing a flatband voltage shift (by  $Q_f$ ) and increased hysteresis (by  $Q_{ot}$ ) by increasing layer thickness is presented.



**Figure 8:** C-V plots of HfO<sub>2</sub> layers deposited at 520 °C with thicknesses of 4, 8 and 16 nm. Figure shows a larger C-V hysteresis and more positive flatband voltage for thicker layers.

## 5. Determination of Flatband Voltage

Flatband voltage is usually described as the built-in potential of MOS device caused by the work function difference between the silicon substrate and metal gate ( $\phi_{ms}$ ) and charges present at silicon surface ( $Q_{it}$ ) and other oxide charges ( $Q_f$ ,  $Q_{ob}$ ,  $Q_m$ ) [16] and for a uniformly doped substrate and the gate voltage is referenced to the grounded back contact can be written as;

$$V_{fb} = \phi_{ms} - \frac{Q_f}{C} - \gamma \frac{Q_m}{C} - \gamma \frac{Q_{ot}}{C} - \gamma \frac{Q_{it}(\phi_s)}{C} \quad (13)$$

where  $\phi_s$  is the surface potential.  $V_{fb}$  can be calculated from (13) if the amount of charges in oxide and at interface and the  $\phi_{ms}$  are known. In practical, a measured C-V

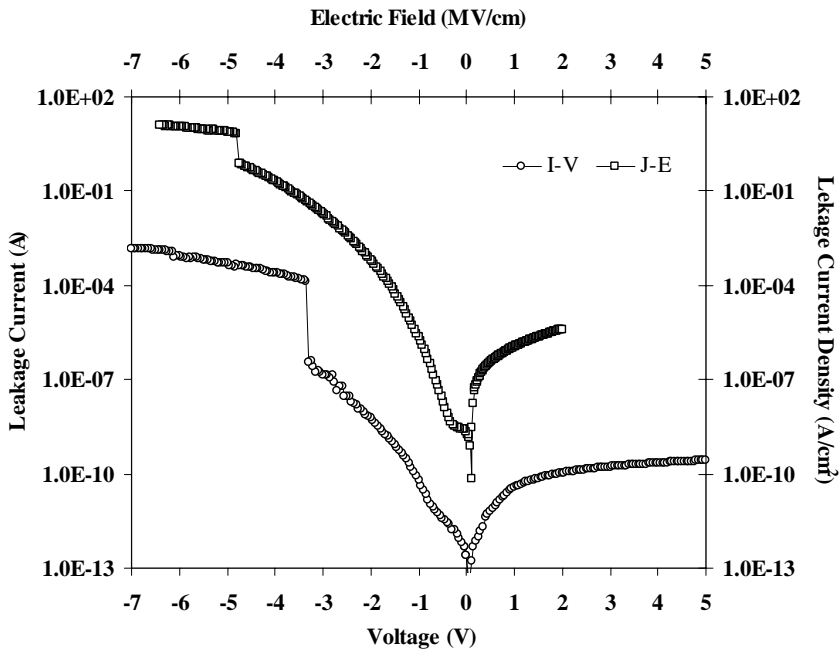
curve is stretched-out due to  $Q_{it}$  and shifted from the theoretical C-V curve by  $Q_f$  and  $Q_m$ . Methods for  $V_{fb}$  determination, listed in literature have major difficulties in the case of high- $k$  dielectrics because of high leakage, high  $D_{it}$  and high oxide charges, which causes stretch-out of C-V curves and considerable amount of  $V_{fb}$  shift by changing oxide thickness. In this work, CVC simulation is used for  $V_{fb}$  determination for practical purposes.

## 6. Determination of Work Function Difference

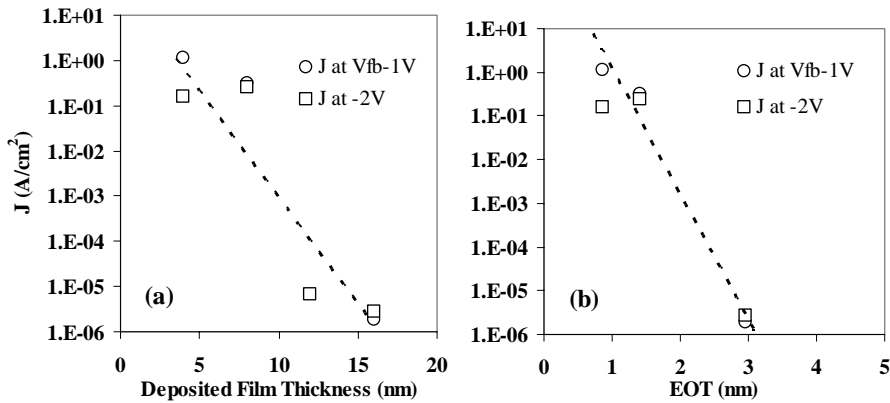
See the 'Determination of Fixed Oxide Charges' section

## 7. Current-Voltage Measurements

$I$ - $V$  Measurements were performed on multiple electrode areas for minimizing errors may be caused by series parasitic resistance [17]. Typical measurement routine consists of sweeping for positive voltages (reverse bias) and then going to negative voltages (forward bias) for p-type MOS structures with a voltage sweeping rate of a 50 mV/s. Subsequently, the measured current is normalized by the electrode area and converted to leakage current density ( $J$ ), whereas the applied bias is transformed to electric field ( $E$ ) using the deposited layer thickness.



**Figure 9:** Difference between  $I$ - $V$  and corresponding  $J$ - $E$  plots of a 4 nm thickness  $\text{CeO}_2$ - $\text{HfO}_2$  laminated dielectric deposited at 520 °C. Leakage current is translated to leakage current density by normalizing the electrode area ( $100 \times 100 \mu\text{m}^2$  in graph).



**Figure 10:** Leakage current densities at 1 V beyond  $V_{fb}$  (open circle) and at -2 V gate voltage (square) are shown versus deposited layer thickness (a) and versus EOT (b) of  $HfO_2$  dielectrics deposited at 520 °C. Dashed lines are guide for eye purpose only.

The difference between deposited layer thickness and total physical thickness (includes interface oxide and deviations in deposited layer thickness) is neglected in presentation of results. Difference between  $I-V$  and  $J-E$  curves are presented in Figure 9. For comparing the leakage current properties of deposited layers, the leakage current density at a given gate voltage is important. This given voltage is usually selected as 1 V beyond flatband voltage, where the MOS device is in accumulation, and/or a fixed voltage which is well above flatband voltage, i.e. -2 V for p-type MOS devices [23]. Both values are presented in this study for a given process condition (i.e. deposition temperature, cooling rate) for observing the effect of layer thickness or for a given layer thickness for comparing the effect of different processing conditions, on leakage current reduction. Figure 10 shows the difference between the leakage current densities versus deposited layer thickness and EOT, for 1 V beyond  $V_{fb}$  and at a given voltage of -2 V.

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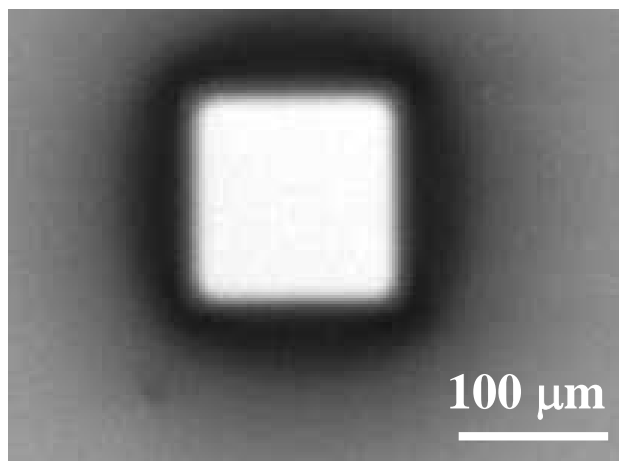


## Appendix 2

### Processing of Au and TaN Electrodes

#### *Au Electrodes*

Au electrodes are deposited at room temperature by sputtering in Ar plasma via a shadow mask. A Perkin-Elmer sputtering system with a load lock is used for deposition. A 2" Si wafer with holes of  $100 \times 100 \mu\text{m}^2$  is used as a shadow mask. Figure 1 show the typical Au electrode deposited via the shadow mask. Note that the electrode size is larger than the size in shadow mask. This is caused by the broadening originated from the distance between the substrate and the mask. Therefore, the electrodes are photographed by SEM (backscattered electron image<sup>7</sup>) after each deposition. SEM images (only the electrode area) then converted to a 2 bit image and the electrode area is calculated by the number of white pixels in the SEM image.



**Figure 1:** SEM image of the Au electrode deposited by sputtering via a shadow mask with  $100 \times 100 \mu\text{m}^2$  holes.

<sup>7</sup> The contrast in the backscattered electron image (BEI) is correlated to the atomic number of the elements present in the photographed area on flat surfaces. Therefore, areas with Au electrodes look bright, whereas the other parts of the surface look darker.

### *TaN Electrodes*

TaN electrodes are deposited at room temperature by sputtering in a Veeco 800 PVD system. A Ta target (300 mm diameter) is sputtered in Ar+N<sub>2</sub> gas mixture at 10 mTorr, with flow rates of 90 and 6 sccm for Ar and N<sub>2</sub>, respectively. TaN layer is then processed by lithography and etching for electrode patterning. Four different electrode areas achieved after the process as 100x100, 200x200, 400x400 and 800x800 μm<sup>2</sup>. The processing steps of lithography and etch are as follows:

1. HMDS primer (4000 rpm 20 s)
2. 1.6 μm Arch 907/17 resist (4000 rpm 20 s)
3. Softbake: 1 min, 95 °C
4. UV-light exposure: 6 s Karl-Suss mask aligner
5. After exposure bake: 1 min 120 °C
6. Development OPD4262 45 s
7. Rinse + spin dry
8. TaN etch: PlasmaTerm 400 (parallel plate) etcher, 44 ml/min CF<sub>4</sub> / 10% O<sub>2</sub> 0.1 mbar +/- 100 W RF power, 5 min
9. Resist strip: Tepla 300 plasma stripper. 10 min 1 kW 500 ml/min N<sub>2</sub> heat-up.  
60 min 1 kW 700 ml/min O<sub>2</sub> strip

Steps 1 - 8: one sample at a time

Steps 9 + 10: batch of 8 samples

# Summary

Since the early years of integrated circuit (IC) technology, the complexity of the IC devices has increased continuously as predicted by the famous Moore's Law. Instead of being a law of physics, this is a self-fulfilling prophecy, which is later formed the basis of the technology development roadmap. As of 2006 most of the central processing units (cpu) are produced at 90 nm level (the size of a transistor in an IC) and even 65 nm devices are recently introduced. For emphasizing the effect of scaling trend it's good to remember that just a decade ago device dimensions were in level of 500 nm. The gate dielectric thickness, which is typically 1/25 of the gate length, is also decreased accordingly to achieve a good channel control, which can be defined by the terms of gate capacitance. The thickness of the state of the art dielectrics (SiO<sub>2</sub> and SiON) are below the tunneling limit and doesn't meet the gate leakage requirements defined in the International Technology Roadmap for Semiconductors (ITRS). High-*k* gate dielectrics are introduced as a solution for overcoming the gate leakage problem by maintaining the same gate capacitance levels. According to the simple parallel plate capacitor relation, the same gate capacitance level can be achieved with a thicker dielectric layer which has a higher dielectric constant than SiO<sub>2</sub> and SiON. Larger physical thickness of the gate dielectric helps overcoming the gate leakage problem. A number of materials have been proposed as high-*k* gate dielectrics on silicon. However, still a manufacturable solution for near term expectations is not found.

A suitable high-*k* dielectric material has to have high permittivity, a large barrier height (~4-5 eV), thermodynamical stability on silicon, high interface quality, gate electrode compatibility, reliability and of course the process compatibility. In the search for a new material with these properties Pulsed Laser Deposition (PLD) is one of the most powerful tools. It has a number of advantages like independent control of process parameters, layer control in the atomic level, ability of using multiple target materials for multilayer depositions and fast processing compared to the other deposition methods makes PLD an attractive tool for materials research. In this work, PLD is used for deposition of CeO<sub>2</sub> and HfO<sub>2</sub> layers. Different processing conditions were investigated from oxidizing to reducing ambient deposition, *in-situ* post deposition anneal, binary oxides as well as the laminated layers of CeO<sub>2</sub> and HfO<sub>2</sub>.

The pre-deposition treatments, *i.e.* native oxide removal and thermal treatment, and deposition conditions are discussed in Chapter 2. It is found that the pre-deposition anneal of hydrogen passivated silicon substrates improves the layer quality and also affects the hydrogen presence in the layers as indicated by secondary ion mass spectrometry (SIMS). Next to the substrate treatment, special emphasis has been given on the use of a reducing ambient followed by an *in-situ* high oxygen pressure post

deposition anneal (PDA). It is shown that the crystalline orientation of CeO<sub>2</sub> layers depends on the ambient conditions: (111) orientation has been found using reducing conditions, whereas the layers grown in oxygen were randomly oriented.

In Chapter 3 the properties of the CeO<sub>2</sub> and HfO<sub>2</sub> binary oxides, are discussed. A thickness series of the layers from 4 to 16 nm were deposited at 420 and 520 °C followed by an *in-situ* PDA with a 5 °C/min cooling rate. Analyses showed that the crystallinity of the layers is thickness dependent. As the layer thickness increases, the layers evolve to a polycrystalline structure with a preferred orientation. This polycrystalline structure alters the electrical properties drastically, increases the leakage current in particular. The best leakage current reduction is achieved by CeO<sub>2</sub> layers deposited at 420 °C with two orders of magnitude lower than SiO<sub>2</sub> reference data. However, 4 nm HfO<sub>2</sub> layers deposited at 520 °C is showed the lowest equivalent oxide thickness (EOT) of 0.95 nm. Fixed charge density ( $Q_f$ ) of the CeO<sub>2</sub> layers in level of  $5 \times 10^{11} \text{ cm}^{-2}$ , is found to be two orders of magnitude lower than HfO<sub>2</sub> layers. The anomaly of the  $k$  value of the CeO<sub>2</sub> layers extracted by the EOT-physical thickness (EOT- $t_{\text{ph}}$ ) plots was attributed to the thickness dependent crystallinity of the layers. Increased crystallinity in thicker layers results in lower EOT values hence reduces the slope of the linear fit on the plot.

Investigating the properties of the laminated structures of CeO<sub>2</sub> and HfO<sub>2</sub>, called as nanolaminates, was the major aim of this work. The basics of the lamination, *i.e.* the layer sequence and the individual layer thickness are presented in the first part of Chapter 4. Effect of the deposition ambient, deposition temperature, cooling rate during *in-situ* PDA, effect of the oxidation time during PDA were discussed. Modification of the Si- high- $k$  interface by depositing a cerium metal interlayer prior to high- $k$  deposition is also given in Chapter 4. It's found that the Si-HfO<sub>2</sub> interface promotes the crystallinity of the layers compared to the Si-CeO<sub>2</sub> interface. Comparison of binary CeO<sub>2</sub> layer with the laminated structure with a Si-CeO<sub>2</sub> interface showed that the lamination diminishes the crystalline phase formation. The crystalline phase formed in the CeO<sub>2</sub>/HfO<sub>2</sub> nanolaminates is likely to be CeHfO<sub>4</sub> according to the fast Fourier transform (FFT) analyses on the transmission electron microscope (TEM) images of the layers. However, one should note that this structure is nearly identical to (111) CeO<sub>2</sub> and HfO<sub>2</sub>. Individual layer thickness on the laminates is found to be affecting the capacitance-voltage ( $C$ - $V$ ) hysteresis of the layers: As the individual layer thickness increases, the  $C$ - $V$  hysteresis increases up to 2 V. This behavior is correlated to the formation of a crystalline phase in the case of increased individual layer thickness in the laminated structure. Investigation of the effect of deposition temperature and different *in-situ* PDA conditions also showed that the layers' properties are strongly depending on their crystallinity and the crystallinity is not only affected by deposition temperature and PDA parameters, but the layer thickness as well. The best leakage current

reduction, almost six orders of magnitude lower than SiO<sub>2</sub> reference data, is achieved by the 4 nm layers deposited at 420 °C and the PDA with a 2 °C/min cooling rate.

Improvement of interface properties by means of cerium metal interlayer showed that the interface oxide thickness didn't improve significantly. However, orientation of the laminated structure is found to be improving by this application. An epitaxial structure on top of the amorphous interface oxide is observed by TEM in the 8 nm laminate with a cerium metal layer deposited at room temperature (RT). The 4 nm laminate grown at 520 °C, with a cerium interlayer deposited at RT gave an EOT of 1.9 nm and a leakage current reduction of six orders of magnitude lower than SiO<sub>2</sub> reference data.

Fabrication of metal oxide semiconductor field effect transistors (MOSFET) with CeO<sub>2</sub>/HfO<sub>2</sub> nanolaminates are presented in Chapter 5. Formation of an upper interface between the high-*k* layer and the aluminum gate electrode was observed. Intensive analyses on the interface showed that the composition is amorphous Al<sub>2</sub>O<sub>3</sub>. A significant aspect of the devices with Al<sub>2</sub>O<sub>3</sub> upper interface was the interface between the silicon substrate and the high-*k* layer, which was in level of a monolayer thickness. This is showed that the Si – high-*k* interface can be reduced by the gate metal to form an upper interface. However, the presence this non-uniform upper interface layer *and* the subsurface defects in the channel region decreased the device performance. Subsequent interface oxide formation during device processing (*i.e.* plasma etching of TaN electrodes) is also given in the final part of Chapter 5.

The details of the techniques used for electrical characterization of the high-*k* layers investigated in this thesis are given in Appendix 1. In Appendix 2, the details of electrode processing for device fabrication are presented.



# Samenvatting

Vanaf de beginjaren van de 'integrated circuit' (IC) -technologie, is de complexiteit van IC devices continu vergroot, zoals voorspeld door de beroemde wet van Moore. In plaats van een natuurkundige wet is dit een zelfontwikkende profetie, welke later de basis vormde van de routekaart voor technologische ontwikkeling. Vanaf 2006 worden de meeste 'central processing units' (cpu) geproduceerd op een 90 nm-schaal (de grootte van een transistor in een IC), terwijl recent zelfs 65 nm-devices zijn geïntroduceerd. Om het effect van schaalverkleining te benadrukken, bedenk dan dat nog geen decennium geleden de device afmetingen in de orde grootte van 500 nm waren. De dikte van het 'gate'-dielectricum, typisch  $1/25^e$  van de gate-lengte, is dienovereenkomstig verkleind om een goede 'channel'-controle te verkrijgen, welke gedefinieerd kan worden in termen van de gate-capaciteit. De dikte van 'state of the art' dielectrica (zoals  $\text{SiO}_2$  en  $\text{SiON}$ ) is kleiner dan de tunnelling-limiet en voldoet niet aan de gate lek-vereisten, zoals gedefinieerd in de 'International Technology Roadmap for Semiconductors' (ITRS). Hoge- $k$  gate-dielectrica worden geïntroduceerd om het gate lek-probleem te overwinnen. Volgens de theorie van een parallelle plaat-capaciteit, kan eenzelfde gate-capaciteit worden bereikt met behulp van een dikker dielectricum met een grotere dielectrische constante dan  $\text{SiO}_2$  en  $\text{SiON}$ . Een fysisch dikker gate-dielectricum helpt het gate lek-probleem te overwinnen. Een aantal materialen is voorgesteld als hoge- $k$  gate-dielectricum op silicium. Echter, een produceerbare oplossing welke voldoet aan de nabije verwachtingen is nog niet gevonden.

Een bruikbaar hoge- $k$  dielectricum moet een hoge permittiviteit, een grote barriere hoogte ( $\sim 4\text{-}5$  eV), een thermodynamische stabiliteit op silicium, een hoge interface kwaliteit, gate electrode compatibiliteit, betrouwbaarheid en processing compatibiliteit hebben. In de zoektocht naar een nieuw materiaal met deze eigenschappen is gepulste laser depositie (PLD) een van de meest krachtige technieken. Het heeft een aantal voordelen, zoals onafhankelijke controle over de proces-parameters, precieze laag-controle op atomaire schaal, de mogelijkheid om meerdere target materialen te gebruiken voor multilaag-deposities, en een hoge proces snelheid. Deze voordelen maken PLD een aantrekkelijke techniek voor materiaalkundig onderzoek, vergeleken bij andere depositie-methodes. In dit werk wordt PLD gebruikt voor de depositie van zowel afzonderlijke, als wel gelamineerde lagen van  $\text{CeO}_2$  en  $\text{HfO}_2$ . Verschillende proces-condities zijn onderzocht, van oxiderende tot reducerende depositie-omgeving en *in-situ* post-depositie annealing.

De pre-depositie behandelingen, *i.e.* verwijderen van native oxides en thermische behandelingen, en depositie-condities worden behandeld in Hoofdstuk 2. Het blijkt dat pre-depositie annealing van waterstof gepassiveerde silicium substraten

de film-kwaliteit verbetert, maar ook de aanwezigheid van waterstof in de film beïnvloedt, zoals aangetoond met ‘secondary ion mass spectroscopy’ (SIMS). Naast de substraat behandeling, is speciale aandacht geschonken aan het gebruik van een reducerende omgeving gevolgd door een in-situ post-depositie anneal (PDA) onder hoge zuurstofdruk. Aangetoond wordt dat de kristallijne oriëntatie van de CeO<sub>2</sub> films afhangt van de omgevings-condities: (111) oriëntatie ontstaat bij reducerende condities, terwijl films gegroeid in zuurstof willekeurig georiënteerd waren.

In Hoofdstuk 3 worden de eigenschappen van de CeO<sub>2</sub> en HfO<sub>2</sub> binaire oxides besproken. Een dikte-serie van films van 4 tot 16 nm zijn gedeponeerd bij 420 and 520 °C gevolgd door een in-situ PDA met een afkoelsnelheid van 5 °C/min. Analyse toonde aan dat de kristalliniteit laagdikte afhankelijk is. Bij een groeiende laagdikte, evolueert de laag in een polykristallijne structuur met een geprefereerde oriëntatie. Deze polykristallijne structuur beïnvloedt de elektrische eigenschappen sterk, in het bijzonder een verhoging van de lekstroom. Van de binaire oxides wordt de sterkste lekstroom-reductie bereikt in op 420 °C gegroeide CeO<sub>2</sub> films welke 2 ordegrottes lager is dan SiO<sub>2</sub> referentie-data. Echter, op 520 °C gedeponeerde HfO<sub>2</sub> films van 4 nm dik lieten de laagste ‘equivalent oxide thickness’ (EOT) zien van 0.95 nm. De ‘fixed charge density’ ( $Q_f$ ) van de CeO<sub>2</sub> films, ordegrutte  $5 \times 10^{11} \text{ cm}^{-2}$ , blijkt 2 ordegrottes lager te liggen dan die van HfO<sub>2</sub> films. De onrealistisch hoge  $k$ -waarde van de CeO<sub>2</sub> films, verkregen uit de EOT-fysieke dikte (EOT- $t_{ph}$ ) plots, wordt toegeschreven aan de dikte-afhankelijkheid van de kristalliniteit van de films. Verhoogde kristalliniteit in dikkere films resulteert in lagere EOT waardes en derhalve verlaagt de helling van de lineaire fit van de plot.

Het onderzoeken van de eigenschappen van gelamineerde structuren van CeO<sub>2</sub> en HfO<sub>2</sub>, ‘nanolaminates’ genoemd, was het hoofddoel van dit werk. De basis van het lamineren, i.e. de laag-volgorde en de individuele laagdiktes, worden uiteengezet in het eerste deel van Hoofdstuk 4. Het effect van de depositie-omgeving, depositie-temperatuur, afkoelsnelheid tijdens in-situ PDA, en de oxidatie-tijd tijdens PDA worden besproken. Het blijkt dat het Si-HfO<sub>2</sub> interface de kristalliniteit van de films bevordert vergeleken met het Si-CeO<sub>2</sub> interface. Vergelijking van een binaire CeO<sub>2</sub> film met gelamineerde structuur met het Si-CeO<sub>2</sub> interface toont aan dat laminering de vorming van een kristallijne fase afzwakt. De kristallijne fase gevormd in het CeO<sub>2</sub>/HfO<sub>2</sub> laminaat is waarschijnlijk CeHfO<sub>4</sub>, volgens de fast Fourier transformatie (FFT) analyses op de transmissie elektronen microscoop (TEM) opnames van de films. Echter, het dient opgemerkt te worden dat deze structuur bijna identiek is aan (111) CeO<sub>2</sub> en HfO<sub>2</sub>. De individuele laagdikte van de laminaten blijkt de capaciteit-voltage ( $C$ - $V$ ) hysteresis van de films te beïnvloeden: Bij een groeiende individuele laagdikte veggroot de  $C$ - $V$  hysteresis tot 2 V. Dit gedrag is gecorreleerd aan de vorming van een kristallijne fase in het geval van vergrote individuele filmdikte. Onderzoek naar het effect van depositie-



temperatuur en verschillende in-situ PDA condities toonde ook aan dat de laag-eigenschappen sterk afhangen van hun kristalliniteit. De kristalliniteit van de films is niet alleen afhankelijk van de depositie-temperatuur en de PDA parameters, maar ook van de filmdikte. De sterkste lekstroom-reductie, bijna 6 ordegroottes lager dan de SiO<sub>2</sub> referentie-data, wordt bereikt door 4 nm films gegroeid op 420 °C en de PDA met een 2 °C/min afkoelsnelheid.

Modificatie van het Si hoge-*k* interface door depositie van een cerium metaal tussenlaag vòòr hoge-*k* depositie wordt ook besproken in Hoofdstuk 4. Verbetering van de interface eigenschappen door middel van een cerium metaal tussenlaag toonde aan dat de interface oxide-dikte nauwelijks verbeterde. Echter, de oriëntatie van de gelamineerde structuur bleek te verbeteren. Een epitaxiale structuur bovenop het amorf interface oxide is waargenomen door TEM in het 8 nm laminaat met cerium metalen film gedeponerd bij kamertemperatuur (RT). Het 4 nm laminaat gegroeid bij 520 °C met cerium tussenlaag gedeponerd bij RT, gaf een EOT van 1.9 nm en een lekstroom-reductie van 6 ordegroottes lager dan de SiO<sub>2</sub> referentie-data.

De fabricage van metaal oxide halfgeleider veld effect transistoren (MOSFET) met CeO<sub>2</sub>/HfO<sub>2</sub> nanolaminates wordt behandeld in Hoofdstuk 5. De vorming van een interface tussen de hoge-*k* film en de aluminium gate-electrode werd waargenomen. Intensieve analyse van dit interface toonde aan dat de compositie amorf Al<sub>2</sub>O<sub>3</sub> is. Een belangrijk aspect van de devices met dit interface was dat het interface tussen het Si substraat en de hoge-*k* film slechts 1 monolaag dikt was. Dit toont aan dat het Si – hoge-*k* interface gereduceerd kan worden door het gate-metaal. De interface oxide vorming tijdens device fabricage (*i.e.* plasma etsen van de TaN electrodes) wordt mede behandeld in Hoofdstuk 5.

De details van de technieken gebruikt voor de elektrische karakterisatie van de onderzochte hoge-*k* films in dit werk zijn gegeven in Appendix 1. In Appendix 2 wordt de synthese van de Au en TaN electrodes voor de MOS devices gepresenteerd.



# *Acknowledgements*

This part of the thesis is one of the hardest to write, I have to admit. None of the words that I know can fully express my gratitude to a number of people, who helped and supported me during my PhD period.

Dave is the person to start with, who helped me from the very first day. I enjoyed very much working with my supervisor Prof. Dave Blank; I learned and experienced a lot in the research environment he created. Besides, spending time with ‘my friend Dave’ was always fun and will always be. I’m grateful to Guus Rijnders, my assistant supervisor, for his guidance and the brilliant ideas he gave me during the discussions we made. Much I owe to Chris Rittersma, who, time and again, helped me to overcome the problems that I faced in my research and taught me a lot about the high- $k$  dielectrics.

Experimental part of this work would be impossible without the help of several people: I’m grateful to Frank Roesthuis for his enormous support in the lab during all my experiments, Lianne Doeswijk for her helps in familiarizing to my work and letting me use the cover picture, Radko Bankras for being ‘my hand’ in the MESA<sup>+</sup> cleanroom (he did really a lot for me), Ton Jenneboer for his precious help in processing the devices that I mentioned in Chapter 5, Henk de Vries and Marcel Weusthof from MESA<sup>+</sup> Test Centrum for their technical support in electrical characterization, Dick Veldhuis, Sybolt Harkema and Gerrit van Hummel for their support in SEM and XRD analyses. I also would like to thank to Andrei Zinine for XPS measurements and to Beatriz Barcones and Rico Keim for making the results clear by TEM analyses.

Apart from the help of the UT team, I also got a big support from Philips Research. It’s my pleasure to thank to Thuy Dao for RBS, Peter Graat for XRD and Jurgen van Berkum, Marcel Verheijen and Monja Kaiser for TEM analyses. I’m also grateful to Jan Verhoeven for several thermal treatments and Jeroen van Zijl for TaN depositions.

I spent half of my PhD period at Low Temperature Division and the other half at the Inorganic Materials Science department. I would like to thank all my colleagues in two groups for the ‘gezellig’ working environment they created. I am indebted to Marion, Ans and Inke, who helped me to survive in the bureaucracy jungle. My officemates (in chronological order) Henk-Jan, Victor, Mark, Seve (rest in peace mate), Aico, Frank! (Also for the Dutch translation of the summary), Matthijn and Paul deserve a big thank you for making the work fun.

I also must thank two men, who shaped my career: Hasan Vezneli has the biggest share in my engineering skills. I learned being creative under any circumstances and utilizing the theoretical knowledge in practice from him. Prof. Dr. Adnan Tekin,

who was my supervisor since my undergraduate, steered me towards science and became a role model to me. I'm grateful for every moment I spent working with him.

Living in a foreign country is always harder than it was in home country. I would like to thank to my friends Caner, Harald, Emrah, Armağan and Çimen, who made my life in Netherlands easier, with their friendship and the joy they brought.

My family, whom I always felt their support during all my education, anytime I needed... Anne ve baba, her ikinize de tüm desteğiniz için çok teşekkürler!

And finally, my best friend, the best travel mate in the world, love of my life, my wife Deniz. Thank you very much for everything you brought in my life. This only has a meaning with you.

## *About the Author*

Koray Karakaya was born on 1<sup>st</sup> of January 1973 in Salihli, Turkey. He lived in Salihli until 1986 when he started high school in Izmir. A year after his graduation from Izmir Atatürk Lisesi in 1989, he started his studies at the Metallurgical Engineering Department at Istanbul Technical University. His graduation project was on high temperature-high pressure synthesis of cubic boron nitride, conducted under the supervision of Prof. Dr. Adnan Tekin.

In 1996 he started his masters education at the Materials Science and Engineering Programme at the Institute of Science and Technology at Istanbul Technical University. He worked on PZT type piezoceramic materials, synthesis and characterization (by XRD and SEM) in particular, supervised by Prof. Dr. Adnan Tekin. Part of his studies has been carried out at Research and Development Institute for Electrical Engineering (ICPE-CA) at Bucharest, Romania.

After he got his master's degree in 1998, he started his PhD studies at the Institute of Science and Technology at Istanbul Technical University. During his studies he worked on developing piezoceramic substrates for surface acoustical wave devices in the frame of a NATO Science for Peace project. When his supervisor Prof. Dr. Adnan Tekin has passed away, he started a new PhD study in 2001 at University of Twente with Prof. Dr. Ing. Dave Blank, at Low Temperature Division and Inorganic Materials Science groups of the Faculty of Science and Technology and MESA<sup>+</sup> Institute for Nanotechnology.

In his studies at University of Twente, he worked on high- $k$  gate dielectric oxides on silicon by pulsed laser deposition, in the project financially supported by Philips. He investigated the properties of CeO<sub>2</sub> and HfO<sub>2</sub> layers, their nanolaminates in particular, for high- $k$  gate dielectric applications and the results are presented in this thesis.



Since the early years of integrated circuit (IC) technology, the complexity of the IC devices has increased continuously as predicted by the famous Moore's Law. As of 2006, most of the central processing units are produced at 90 nm level and even 65 nm devices are recently introduced. The thickness of the gate dielectric is also decreased accordingly for a good channel control, which can be defined by the terms of gate capacitance. The thickness of the state of the art dielectrics are below the direct tunneling limit and doesn't meet the near future gate leakage requirements defined in the International Technology Roadmap for Semiconductors. High-*k* gate dielectrics are introduced as a solution for overcoming the gate leakage problem by maintaining the same gate capacitance levels with larger physical thicknesses.

In the search for a high-*k* material Pulsed Laser Deposition is one of the most powerful tools. It has a number of advantages like independent control of process parameters, layer control in the atomic level, ability of using multiple target materials for multilayer depositions and fast process compared to the other deposition methods, which make PLD an attractive tool for materials research.

In this thesis, PLD is used for deposition of CeO<sub>2</sub> and HfO<sub>2</sub> layers. Different processing conditions were investigated from oxidizing to reducing ambient deposition, *in-situ* post deposition anneal and deposition of binary oxide layers, as well as the nanolaminates. The electrical and structural properties of the deposited layers were characterized and the links between these properties were tried to be established.

